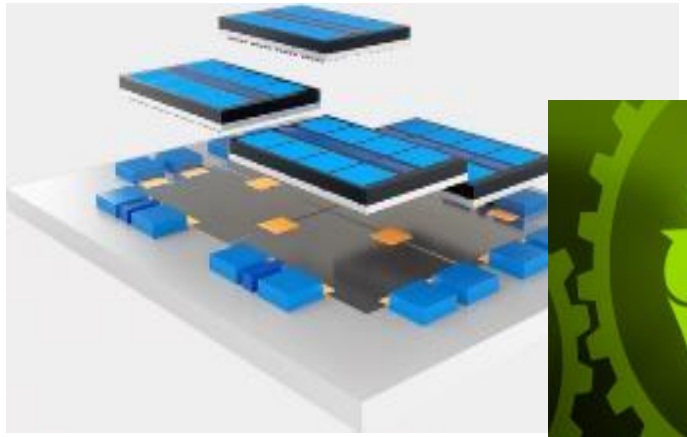
Semiconductor Research Corporation

Because the future can't wait, we bring the best minds together to achieve the unimaginable

Packaging (PKG) and Environment, Safety, and Health (ESH) Research Program Annual Review

June 3-7, 2024
Intel, Chandler, AZ

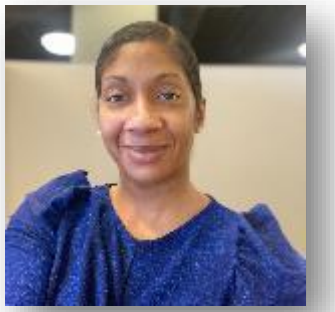


John Oakley, Science Director
Kashyap Yellai, Program Manager
LaDonya Dooley, Research Program Coordinator
Syd Williams-Black, Research Program Coordinator

https://www.src.org/calendar/e007869/

On Behalf of the SRC, Thank You!

- To all the industry members for their sponsorship and mentorship
- To all the Principal Investigators & their Students for the great research effort
- To LaDonya Dooley and Syd Williams-Black at SRC for the logistical support
- To all of you for being in-person with us!



LaDonya Dooley
Program Coordinator
laDonya.dooley@src.org

Sydney “Syd” Williams-Black
Program Coordinator
Syd.Williams-Black@src.org

Thanks for Intel to host PKG + ESH Annual Review !

Dr. Ravi Mahajan
Intel Fellow and
Director of Pathfinding for Assembly and Packaging technologies

SMART-USA Participants Growth of Supporters

- Currently 85+ participants on SRC's MMUSAI proposal team

- Any help with recruiting companies & universities is greatly appreciated
  - Please share Steve.Czarnecki@src.org email to prospective members

> As a well-established center of gravity for transformative research and innovation across the semiconductor ecosystem, SRC is ideally positioned to advance digital twin technology that will strengthen our industry. SIA strongly endorses SRC's proposal for the SMART USA Institute, and we look forward to serving as a partner to SRC, government leaders, and other stakeholders to move this important initiative forward.

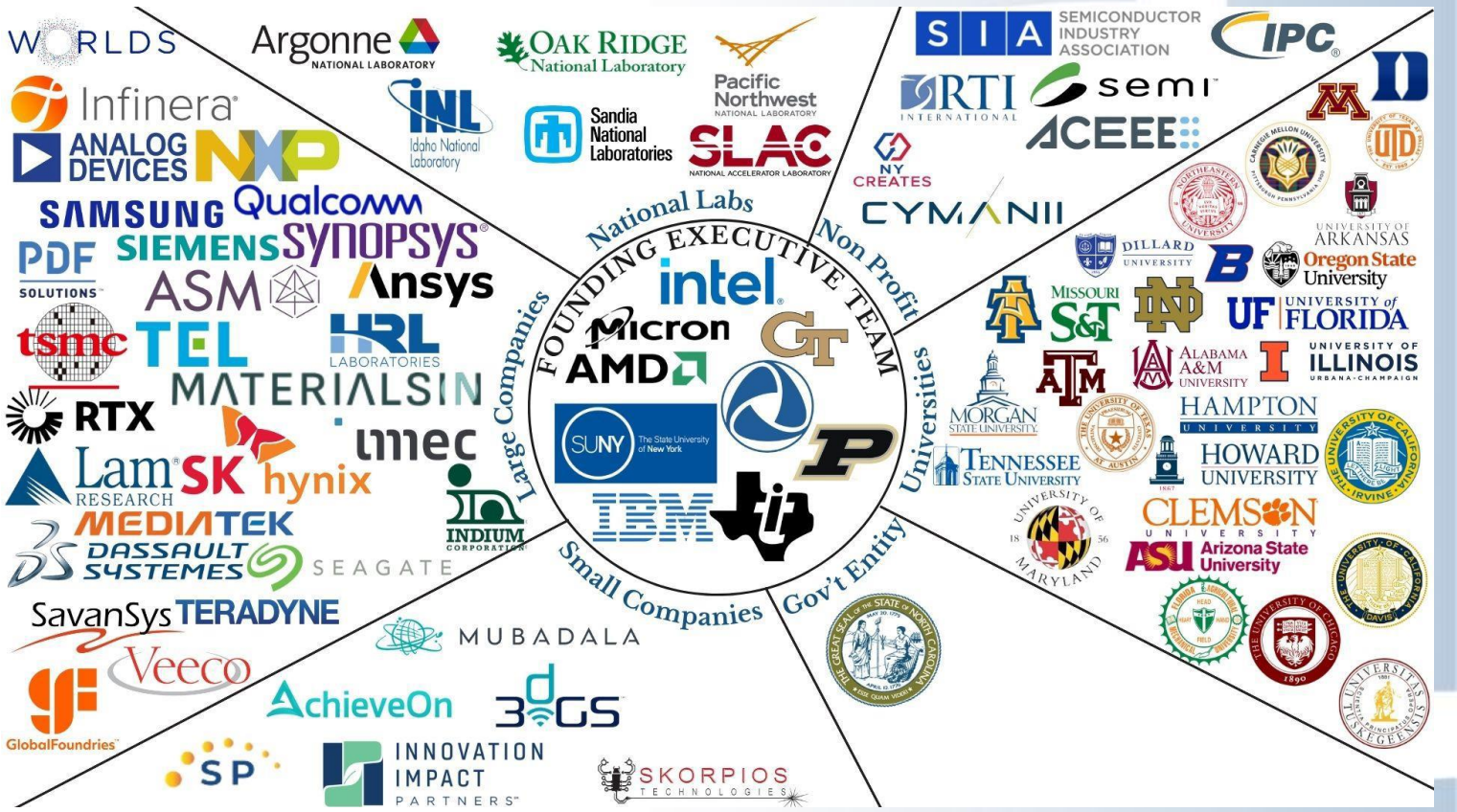
John Neuffer, President & CEO, Semiconductor Industry Association

> SEMI is pleased to partner with SRC to serve the national mission and bring the combined strength of the 2 organizations to bear in the development of a Digital Twin manufacturing innovation institute.

Ajit Manocha, President and CEO of SEMI

> At Purdue, it's full speed ahead with SRC to re-energize semiconductor manufacturing in the USA!

Mung Chiang, President, Purdue University



SRC

https://www.src.org/about/smart-usa-institute/

Annual Review Reminders

Everyone participating in-person (remote is listen only)

Presenters should remember to speak clearly and keep within the allotted time.

Timing:
30 min (25 min presentations)

Presentations and Q&A will be live. Please be mindful, so watch the time to leave 5 minutes for Q&A!!!

Informal Presentations

Please indicate if you want the audience to interrupt with questions. Q/A will occur at the end.

Pillar Science, Scholar Recruitment, Liaison Calls & Payments

PILLAR SCIENCE

Project Management

All project leaders and participants should log into Pillar Science and keep the project updated

https://app.pillar.science/news

Project leaders manage their own teams of academics

Industry will join as liaisons to interact on your project

Identify Research Scholar (s)

Project leaders assign research scholars which participate on the project start date including ones not directly sponsored by SRC

SRC may withhold payments if no scholar is assigned

Add scholars to research team and appropriate project in Pillar Science – guidelines

2030 Broadening Participation Pledge

Schedule Liaison Call

Schedule regular calls with industry liaisons at every 4 to 8 weeks cadence, initiated by the university

Scholar participation is encouraged

The university researchers own the interaction format and frequency of these meetings

Regular invoicing

Invoice on regular basis: monthly is preferred

Excess money (calendar year) is considered profit and taxable!

Spending must occur within contract period

Invoicing expected to be at or above 95% invoiced at end of each contract period

Final invoice within 60 days after project ends

No cost extensions (NCE) are not allowed

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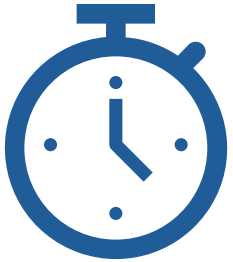
Deliverables, Publications, and Patents



Submit deliverables on time:
even 1 day is too late!

System will flag delinquencies

Late deliverables will stop invoices being paid and can jeopardize future funding

Contact SRC if there are issues with getting deliverables on time

All submissions will be done in Pillar Science

Pre-publication drafts with Supporting Data (see backup slide for guidance) must be deposited at SRC > 60 days before published

Best practice: deposit draft to SRC website when submitting to journal/conference (also thesis)

Update the draft on the SRC website with final paper after acceptance (select submit a new version)

Acknowledgement of SRC funding must be added to all publications

At minimum, the acknowledgement should read: "This work was supported in part by Semiconductor Research Corporation (SRC)."

Patents

Don't forget patents, submit disclosures to SRC if applicable

If approved, SRC does support and pay for the filing for your university

https://www.src.org/about/contracts-ip/#ip

Universities own IP generated by these project and provide non-exclusive royalty free rights to supporting members

Send News Items to SRC

- Send noteworthy events and announcements that you and your team are involved to SRC
- Send this information on a monthly basis using the link https://www.src.org/newsroom/submit/
- We use what we can in our SRC newsletter and monthly emails to the Advisory Board and liaisons
  - Best Paper Awards (who, award, title of piece, where, when and photos of students/faculty)
  - Papers, posters presentations, and/or conference talks
  - Professional Recognition Awards: IEEE, teaching awards, etc.
  - Professional activities such as workshops, tutorials, and invited talks
- All submissions must have a web link (URL) to the award, paper, etc.
  - If you have your own website that contains information pertaining to your research, share the link with SRC as well

More Than 17,000 subscribers!!

https://www.src.org/newsroom/newsletter/

SRC Student Platform on LinkedIn

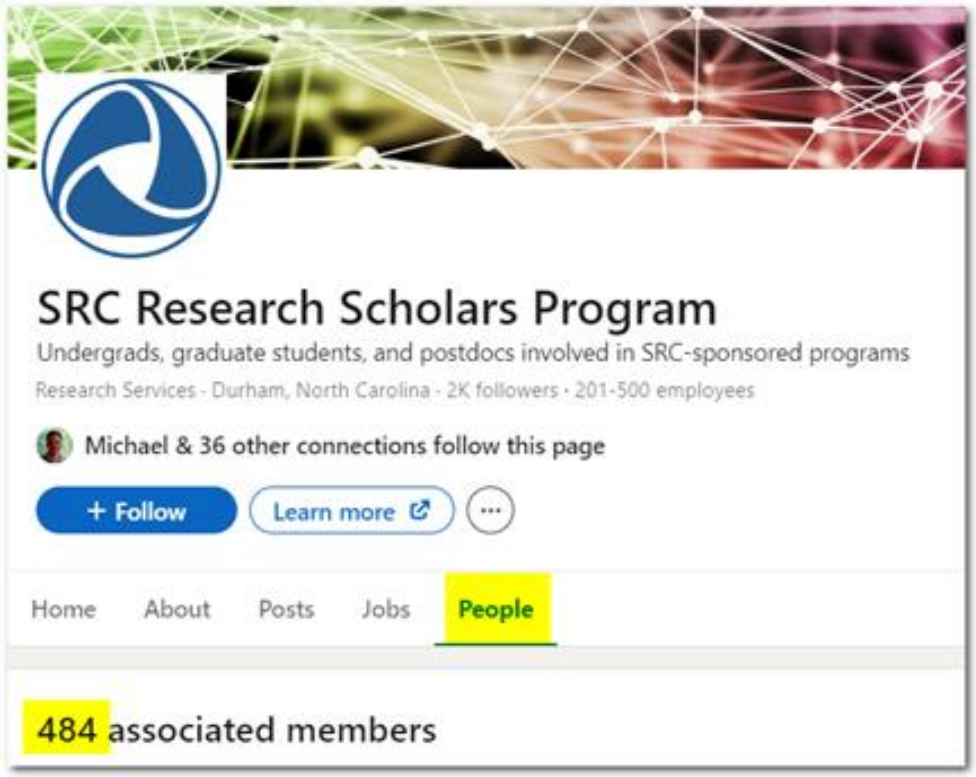
- What is the **SRC Research Scholars Program**?
  - SRC provides undergrads, graduate students, and postdoctoral researchers with a unique education consisting of traditional course work, cutting-edge research, and direct interaction with the semiconductor industry
  - These Research Scholars work on industry-relevant research with SRC-funded faculty who are recognized experts in their fields
  - Through our extensive community of academics and industry personnel, we nurture the evaluation of the talent pipeline for our industry and beyond
  - Our alumni have become industry leaders and renowned faculty researchers, creating a virtuous cycle where mojo begets mojo

Join Now!

SRC encourages all undergrads, graduate students, and postdoctoral researchers to join this program!!!

https://www.src.org/student-center/handbook/linkedin/

Grow SRC Research Scholars LinkedIn to >70% of active scholars and >1k Alumni



SRC supported Researchers (Past and Present):

- Please go join SRC Research Scholar Program on LinkedIn, so we can grow research scholars by 70%
- Also tell Alumni to mark past work experience to get >1K Alumni

https://www.src.org/student-center/handbook/linkedin/

Key Performance Indicators (KPI) Process

PILLAR SCIENCE

https://www.src.org/src/guide/kpi/

Blank KPI forms On Pillar Science	PIs fill out KPI forms As part of Annual Review	SRC perform qualify control on KPI Forms	Industry verify technology transfers (TTs) + report to SRC	TT Master counts summarized in annual report

KPIs have been moved to Pillar Science collaborative workspace

Benefits:

- One-stop shop
- KPI process is visible to SRC members
- Quick recognition of meaningful Technology Transfers

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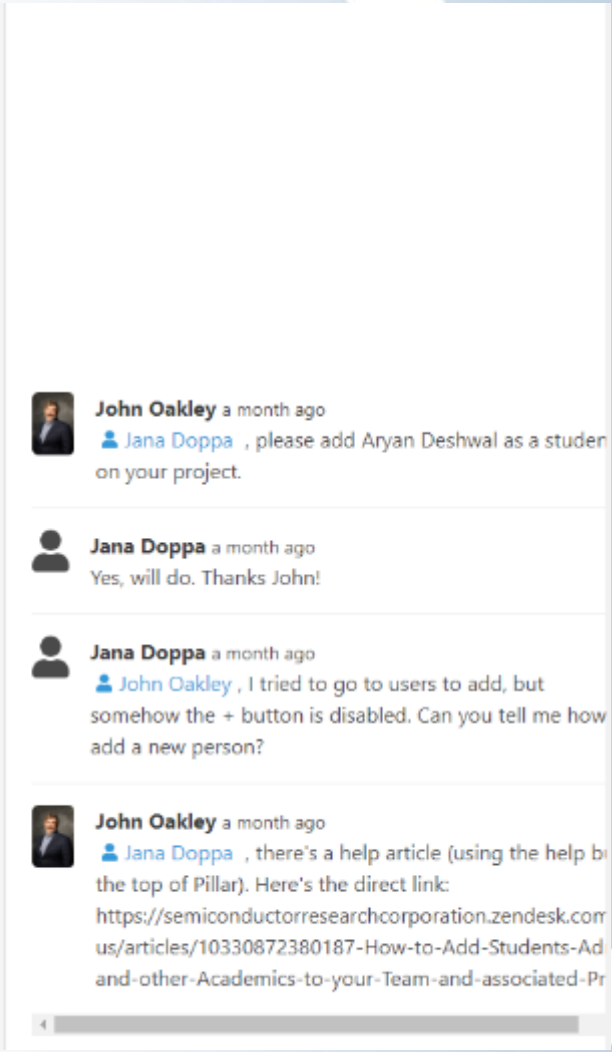
https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/15056064943771-How-to-edit-and-manage-your-Key-Performancer-Indicators-KPI-card-

KPI Best Practices

Informational Video

Example @Mentions Working for KPI Quality Control

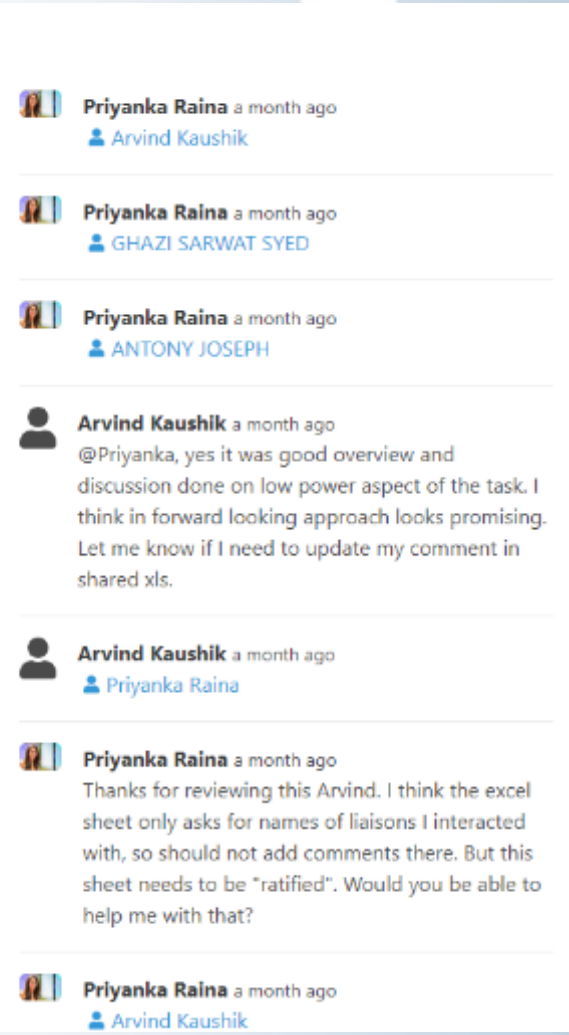
Semiconductor Research Corporation		Project ID	Project Leader	Af
		3014.001	Jana Doppa	Wa
	Your Goals	A Novel Imitation Learning Framework for Self-Optimizing Computing Systems	Intel, Qualcomm, Media Tek	Mike Kish Jain, Qu C
Most Valuable (max 5 pts/each row) - Enter information for current project year				
Demonstrate Viability	Accomplish key program goal; Proof(s) of concept	Problem Addressing: dynamic resource management in mobile SoCs and large manycore systems. Novel Solution: Learning-to-search framework for known applications and Uncertainty-aware online learning for unknown applications. Impact vs. SotA: Significant improvements over prior RL and IL methods in terms of energy savings and overhead reduction.	Working closely with Mike Kishinivesky and Raid Ayoub from Intel on DRM problems.	Mike Kishnive
Set a New Direction – Internal to Member or Externally	Knowledge transfer with examples: Start-up adoption of Arch/SW, Start-up Pathfinding or VC investment, new internal projects at Member (including new products) or decisions to drop existing products/technology/projects; Driving more diverse teams / student base	Problem Addressing: 1) Automating the search for expert policies required for IL. 2) Quantifying uncertainty for online learning for unknown applications. Novel Solution: 1) Constrained Bayesian optimization with pruning using power and performance models. 2) Conformal prediction for theoretically valid predictions from ML models. Impact vs. SotA: Improved accuracy of IL based DRM policies .	Working closely with Mike Kishinivesky and Raid Ayoub from Intel on DRM problems.	Mike Kishnive
Identified Showstopper/ or Mitigation of High Risk	Description and impact; Potential Outcome, Success, or Failure	Problem Addressing: Quantifying uncertainty of DRM policy using ML models was not accurate, which impacted the accuracy of online learning. Novel Solution: Conformal prediction for theoretically-sound and valid predictions from trained ML models Impact vs. SotA: Improved accuracy of ML models through online learning and reduced overhead.	Working closely with Mike Kishinivesky and Raid Ayoub from Intel on DRM problems.	Mike Kishnive
	Code, data, design sets and bigger technology transfers; usage/citation of SRC-sponsored publications by papers	Multiple papers published and submitted in collaboration with Intel Liasions on ML for dynamic	Working closely with Mike	



https://app.pillar.science/datasets/189723

Example KPI's with Vetting Process using @Mentions

	A	B	C	D	
1	Semiconductor Research Corporation		**Project ID**	**Project Leader**	**Afi**
2			**3158.001**	**Priyanka Raina**	
3		**Your Goals**	**Project Title: Hardware Accelerator for Enabling High-Performance AI on Tiny Edge Devices**	**Your Member Interactions (e.g. Intel, TI, etc.)**	**Your Mem of Me**
4	**Most Valuable (max 5 pts/each row) - Enter information for current project year**				
5	**Demonstrate Viability**	Accomplish key program goal; Proof(s) of concept	Problem Addressing: Inference and training of transformer models on edge devices with small amounts of memory. Novel Solution: (1) A DNN accelerator with 8-bit posit datapath for efficiency without compromising accuracy, (2) dynamic power-gating of RRAM banks, (3) posit based transformer inference and training algorithm. Impact vs. SotA: Initial results show that we can train MobileBERT with 8b posit and achieve iso-accuracy as BFloat16.		
6	**Set a New Direction – Internal to Member or Externally**	Knowledge transfer with examples: Start-up adoption of Arch/SW, Start-up Pathfinding or VC investment, new internal projects at Member (including new products) or decisions to drop existing products/technology/projects; Driving more diverse teams / student base	It has been 4 months since the start of this 3 year project, so the research is not complete enough yet to set a new direction in a company.		
7	**Identified Showstopper/ or Mitigation of High Risk**	Description and impact; Potential Outcome, Success, or Failure	None		
8	**Technology Transfers: Adoption at a Member, including government agencies**	Code, data, design sets and bigger technology transfers; usage/citation of SRC-sponsored publications by papers published by members	None so far, we have a software implementation of posit based inference and training of MobileBERT. We will release it as open-source code after testing it on a larger set of transformer networks.		
9	**Fulltime Hire into Member**	Hires & names of hires into Member w/ associated diversity info **(be sure to include Company Names and start dates)**	None so far, the students working on this project have not graduated yet.		
10	**Moderately Valuable (max 3 pts/each row) - Enter information for current project year**				
11	**Transfer from Member to Academia or Start-up**	External use of technology or curriculum	None		
12	**Member Awareness / Collaborations**	Increased number of liaisons that are engaged in project: name and engagement description; Recognizing key liaisons with Mahboob Khan nominations	Interacted with 3 new liaisons, 2 from NXP and 1 from IBM from Jan - Apr 2023, gave them a project overview and discussed potential applications of this work.	NXP Semiconductors, IBM	Arvind Kaushik Ghazi Sarwat S
13	**Cross-Task Awareness / Collaborations**	Evidence of rich exchange, co-authorship, or cross-tasks integrator efforts between PIs	This proposal has only 1 PI responsible for all the tasks, so this is not applicable.		
14	**Ecosystem Development**	#Software releases, setting conference agenda, other evidence of meaningful influence	We will be releasing open-source software for both the hardware design and the posit based algorithms later this year.		



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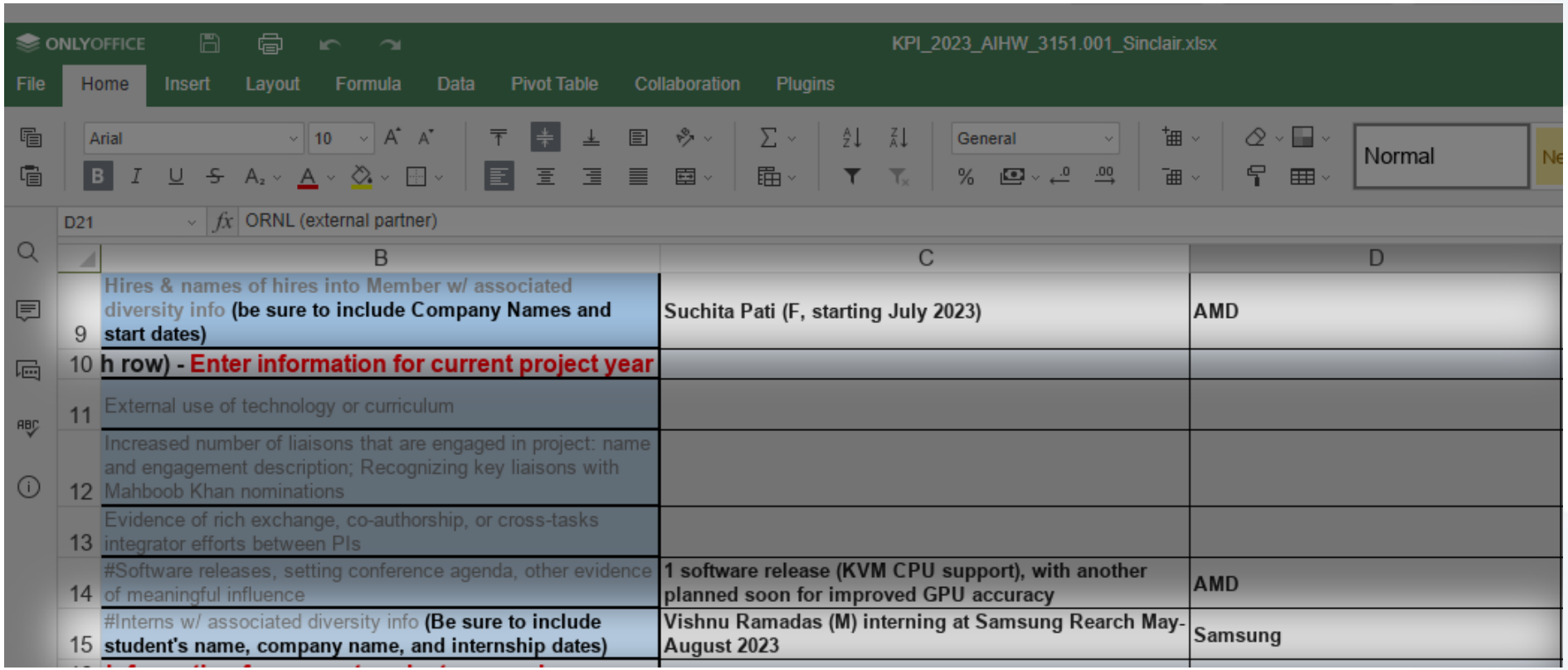
https://app.pillar.science/datasets/189765

Need to have to accurate scholar information in Pillar including Internship and Fulltime Hires



	B	C	D
9	Hires & names of hires into Member w/ associated diversity info **(be sure to include Company Names and start dates)**	Suchita Pati (F, starting July 2023)	AMD
10	**h row) - Enter information for current project year**		
11	External use of technology or curriculum		
12	Increased number of liaisons that are engaged in project: name and engagement description; Recognizing key liaisons with Mahboob Khan nominations		
13	Evidence of rich exchange, co-authorship, or cross-tasks integrator efforts between PIs		
14	#Software releases, setting conference agenda, other evidence of meaningful influence	**1 software release (KVM CPU support), with another planned soon for improved GPU accuracy**	AMD
15	#Interns w/ associated diversity info **(Be sure to include student's name, company name, and internship dates)**	**Vishnu Ramadas (M) interning at Samsung Rearch May-August 2023**	Samsung

Please have clear description →of Full-time and Internship from SRC member companies On Pillar Science

Also, encourage your scholars to include these work experience in their student profiles.

https://app.pillar.science/datasets/189751

Intellectual Property Statement

- The information provided by researchers during this annual review
  - Is the property of the university and of the researchers presenting this information
  - May include research results sponsored by and provided to the funding members
  - May include intellectual property rights belonging to the university and SRC, to which sponsors may have license rights

- By attending or viewing this review, you are agreeing
  - Not to use this information for purposes unrelated to the review unless and until approved by SRC
  - To keep this information in confidence until the university and SRC have evaluated and secured any applicable intellectual property rights

- After any intellectual property rights have been secured, the SRC encourages the University and researchers to publish and freely disseminate this information and results of the sponsored research program.
  - Worldwide patent rights are waived if publication or public dissemination occurs prior to filing a corresponding U.S. provisional or utility patent application

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https://www.src.org/about/contracts-ip/#ip

General Data Protection Regulation

- Applies to SRC
- Personal data regulations
- Involves privacy notices, consent, and security
- SRC Privacy Policy

https://www.src.org/app/account/guide/privacy-policy/

Agenda – Day 1

- Presentations (30 minutes)
  - 25-minute presentations
  - With 5-minute Q&A (live)

All Times local to AZ

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15939665

ESH / PKG Day 1: June 3rd, 2024

Time	Title	Speaker
8:00 AM	**Breakfast**	
8:30 AM - 8:45 AM	**SRC Introduction**	John Oakley SRC
8:45 AM - 9:15 AM	3076.001: A Novel RDL Interposer Fabrication by Low Temperature Hybrid Bonding Method	Kuan-Neng Chen National Yang Ming Chiao Tung Universities
9:15 AM – 9:45 AM	2810.091: Development of Two-Photon Absorption Laser System for Creating Single Event Effects	Robert Baumann University of Texas at Dallas
9:45 AM – 10:15 AM	2878.017: In Situ Studies on Thermal Compression Bonding of Nanotwinned Cu with Passivation Layers	Xinghang Zhang Purdue University
10:15 AM – 10:30 AM	**Break**	
10:30 AM – 11:00 AM	2878.018: Printed Conformal Metal Films for Electromagnetic Interference (EMI) Protection	Paul Chiarot Binghamton University - SUNY
11:00 AM - 11:30 AM	2878.019: High Thermal Interface Conductance Metrology	Amy Marconnet Purdue University
11:30 AM – 12:00 PM	2878.021: Microalloying for Stable Low Temperature Solder Microstructures and Reliable Heterogeneous Integration	John Blendell Purdue University
12:00 PM – 1:30 PM	**Lunch / Poster Session**	
1:30 PM – 2:00 PM	**Industry talk – Ravi Mahajan / Intel**	
2:00 PM – 2:30 PM	2878.020: Intra-Die Cooling of Monolithic 3D Stacks using Oscillating Heat Pipe Spreaders	Liang Pan Purdue University
2:30 PM – 3:00 PM	2878.026: Co-design Scheme for Thermal Management with Backside Power Delivery for High-Power 3D Packages	
3:00 PM – 3:15 PM	**Break**	
3:15 PM – 3:45 PM	2878.022: Interactions Between Electromigration and Fatigue of Regular and Low Temperature Solder Joints	Peter Borgesen Binghamton University - SUNY
3:45 PM – 4:15 PM	2878.028: Optimizing Reliability of Solder Joints Reflowed at Temperatures Below 140C	
4:15 PM - 4:30 PM	**Break**	
4:30 PM – 5:30 PM	TAB CAUCUS AS NEEDED – TAB MEMBERS ONLY	
5:30	**END OF DAY 1**	

https://www.src.org/calendar/e007869/

Agenda – Day 2

- Presentations (30 minutes)
  - 25-minute presentations
  - With 5-minute Q&A (live)

All Times local to AZ

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ESH / PKG Day 2 : June 4th, 2024

Time	Title	Speaker
8:00 AM	**Breakfast**	
8:30 AM - 8:45 AM	**SRC Introduction**	John Oakley SRC
8:45 AM - 9:15 AM	2878.023: Interfacial Adhesion and Strength of Ultrathin Films Using Organic Monolayer Induced Surface Stress	Srinivasan Chandrasekar Purdue University
9:15 AM – 9:45 AM	2878.024: Electromigration Failure in Sn Solder Joints	Marisol Koslowski Purdue University
9:45 AM – 10:15 AM	2878.025: Thermomechanical Reliability Investigation of Barrier/Liner/Seed Layer Options for Nanoscale TSV (< 1 μm)	Tiwei Wei Purdue University
10:15 AM – 10:30 AM	**Break**	
10:30 AM – 11:00 AM	3080.001: Low-temperature Cu-Cu Hybrid Bonding for Die-to-Wafer Application	Chih Chen National Yang Ming Chiao Tung Universities
11:00 AM - 11:30 AM	3070.001: 2.5D Integrated GaN Voltage Regulator (VR) with Embedded Magnetics	Fang Luo State University of New York at Stony Brook
11:30 AM – 12:00 PM	3071.001: Innovation of Warpage Prediction for Transfer Molding and Compression Molding Processes	Bongtae Han University of Maryland, College Park
12:00 PM – 1:30 PM	**Lunch / Poster Session**	
1:30 PM – 2:00 PM	3072.001: PMIP: Power-Magnetics-in-Package Technology for Ultra-Compact Vertical 48V-1V CPU Voltage Regulators	Minjie Chen Princeton University
2:00 PM – 2:30 PM	3073.001: Integrated Chiplet-Encapsulation for 3D Heterogeneous Integration	Muhannad S. Bakir Georgia Institute of Technology
2:30 PM - 3:00 PM	3074.001: High Performance Copper-Epoxy Interfaces for High Frequency Inter-die and Off-package Signal Transmission	John Flake Louisiana State University
3:00 PM – 3:15 PM	**Break**	
3:15 PM – 3:45 PM	3075.001: Advanced Characterization Techniques for Investigating Failure Mechanism of Silicon and Package Interconnects	Choong-Un Kim University of Texas at Arlington
3:45 PM – 4:15 PM	3179.001: Enabling Electromigration Solver for Solder Joint with Various Packaging Structures and Alloys	
4:15 PM - 4:30 PM	**Break**	
4:30 PM – 5:30 PM	TAB CAUCUS AS NEEDED – TAB MEMBERS ONLY	
5:30	**END OF DAY 2**	

https://www.src.org/calendar/e007869/

Agenda – Day 3

- Presentations (30 minutes)
  - 25-minute presentations
  - With 5-minute Q&A (live)

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ESH / PKG Day 3 : June 5th, 2024

Time	Title	Speaker
8:00 AM	**Breakfast**	
8:30 AM - 8:45 AM	**SRC Introduction**	John Oakley SRC
8:45 AM - 9:15 AM	2810.080: Efficient and High-Density Fully In-Package GaN-Based High-Ratio DC-DC Converters	Cheng Huang Iowa State University
9:15 AM – 9:45 AM	3079.001: Characterization of Interfacial Adhesion under Cyclic Loading	Rui Huang University of Texas at Austin
9:45 AM – 10:15 AM	3183.001: Characterization of Interfacial Adhesion over Small Surface Areas	Kenneth Liechti University of Texas at Austin
10:15 AM – 10:30 AM	**Break**	
10:30 AM – 11:00 AM	2878.027: Experimental Characterization of Thermal Shadowing Effect and AI Driven (deep learning) Optimization of Boiling Enhancement Coatings for Single- and Two-phase Immersion Cooling	Bahgat Sammakia Binghamton University - SUNY
11:00 AM - 11:30 AM	3081.001: 2.5D Polymer-based Interposer Technology for the Heterogeneous Integration of 6G Wireless Communication Systems	Yu-Ting Cheng National Yang Ming Chiao Tung Universities
11:30 AM – 12:00 PM	3180.001: AI-Assisted Design-on-Simulation Technology for Advanced Packaging	Kuo-Ning Chiang National Tsinghua University
12:00 PM – 1:30 PM	**Lunch / Poster Session**	
1:30 PM – 2:00 PM	3181.001: Electromigration Research for Flip-Chip, Hybrid, and 3-D Packaging	Dryver Huston University of Vermont
2:00 PM – 2:30 PM	3184.001: High-Capacity, Low-Cost, 100-250GHz Wireless and Waveguide Interface Packages	Mark Rodwell University of California, Santa Barbara
2:30 PM - 3:00 PM	3185.001: Electrodeposition of High Moment-High Resistivity CoFeX (X=P, O) Alloys for Inductor Application	Stanko R. Brankovic University of Houston
3:00 PM – 3:15 PM	**Break**	
3:15 PM – 3:45 PM	3186.001: Socketable BGAs by Surface-Modification of Solder Spheres with Bi-Based Coatings	Vanessa Smet Georgia Institute of Technology
3:45 PM – 4:15 PM	3187.001: Optical DAC-based 64QAM Transmitters in a Silicon-Interconnect-Fabric 3D Package	Sajjad Moazeni University of Washington
4:15 PM - 4:30 PM	**Break**	
4:30 PM – 5:30 PM	TAB CAUCUS AS NEEDED – TAB MEMBERS ONLY	
5:30	**END OF DAY 3**	

https://www.src.org/calendar/e007869/

Agenda – Day 4

- Presentations (30 minutes)
  - 25-minute presentations
  - With 5-minute Q&A (live)

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ESH / PKG Day 4: June 6th, 2024

Time	Title	Speaker
8:00 AM	**Breakfast**	
8:30 AM - 8:45 AM	**SRC Introduction**	Kashyap Yellai SRC
8:45 AM - 9:15 AM	3188.001: Integrated Power Delivery Methodology for 3D ICs	Boris Vaisband McGill University
9:15 AM – 9:45 AM	3195.001: Physics Informed Active Learning for Electrical Analysis of Second Level Interconnects	Ahmet Durgun Middle East Technical University
9:45 AM – 10:15 AM	3196.001: Developing Nanogranular Laminates: An Efficient Soft-magnetic Material for Sub-GHz Power Inductors	Ranajit Sai Tyndall National Institute
10:15 AM – 10:30 AM	**Break**	
10:30 AM – 11:00 AM	3078.001: Tunable Low-cost Passivation Coating for Facilitating Copper Wafer-level Bonding	Oliver Chyan University of North Texas
11:00 AM - 11:30 AM	3182.001: Tunable Thermal Conductivity, Dielectric Strength Biobased Molding Compounds and Die-Attach Adhesives	Nandika A. D'Souza University of North Texas
11:30 AM – 12:00 PM	3233.001: Exploring Deep Eutectic Solvents as Environmentally Benign Post-etch Residue Removers	Hao Yan University of North Texas
12:00 PM – 1:30 PM	**Lunch / Poster Session**	
1:30 PM – 2:00 PM	**Industry talk – Dave Speed / Global Foundries**	
2:00 PM – 2:30 PM	3077.001: Predictive-Models and Characterization-Data for Package-Interfaces under Sustained High-Temperature High-Humidity Operation in Automotive Underhood Environments	Pradeep Lall Auburn University
2:30 PM – 3:00 PM	3232.001: Sustainable non-PFAS Packaging Materials Process-Performance-Reliability Interactions	
3:00 PM – 3:15 PM	**Break**	
3:15 PM – 3:45 PM	3096.001: Evaluating Alternative and Environmentally Friendly Etchants and Processes	Jane Chang University of California, Los Angeles
3:45 PM – 4:15 PM	3099.001: Addressing Emission Challenges through Exhaust Monitoring and Control	
4:15 PM - 4:30 PM	**Break**	
4:30 PM – 5:30 PM	TAB CAUCUS AS NEEDED – TAB MEMBERS ONLY	
5:30	**END OF DAY 4**	

https://www.src.org/calendar/e007869/

Agenda – Day 5

- Presentations (30 minutes)
  - 25-minute presentations
  - With 5-minute Q&A (live)

All Times local to AZ

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ESH / PKG Day 5 : June 7th, 2024

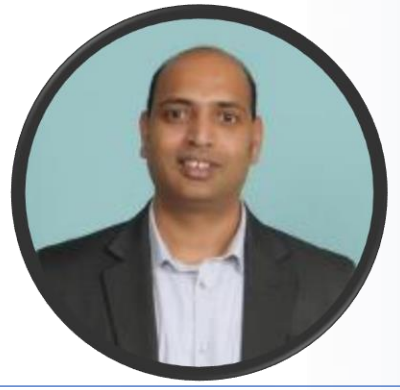
Time	Title	Speaker
8:00 AM	**Breakfast**	
8:30 AM - 8:45 AM	**SRC Introduction**	Kashyap Yellai SRC
8:45 AM - 9:15 AM	**3100.001**: Environmentally Benign Chemical Mechanical Planarization Slurries Aided by Amino Acids	Jihoon Seo / Clarkson University
9:15 AM – 9:45 AM	**3101.001**: Plasma-based Treatment of Per- and Polyfluoroalkyl Substances (PFAS)	Selma Mededovic / Clarkson University
9:45 AM – 10:15 AM	**3244.001**: Studies of PFAS Free Non-ionic Photoacid Generators and Photoresists for Benign EUV Lithography	Christopher K. Ober / Cornell University
10:15 AM – 10:30 AM	**Break**	
10:30 AM – 11:00 AM	**3230.001**: Combining Closed-circuit Nanofiltration with Adsorbents to Meet Stringent PFAS Treatment Requirements for Semiconductor Fabrication Wastewater Effluent	Timothy Strathmann / Colorado School of Mines (Remote)
11:00 AM - 11:30 AM	**3228.001**: Experimental Evaluation of Degradation Rates and Transformation Products of Fluorinated Polymers used During Semiconductor Manufacturing	Damian Helbling / Cornell University
11:30 AM – 12:00 PM	**3229.001**: Targeted Sampling and Analysis to Support Source Tracking and Mass Balances of Organofluorine-Containing Compounds in Semiconductor Manufacturing Facilities	
12:00 PM – 1:30 PM	**Lunch / Poster Session**	
1:30 PM – 2:00 PM	**3231.001**: Light Responsive Poly(olefin sulfone)s for PFAS-free Photoresists with Dry Development and Stripping	John Matson / Virginia Polytechnic Institute and State University
2:00 PM – 2:30 PM	**3245.001**: Distributed Wastewater Surveillance Platform Leveraging Scalable Hybrid Microfluidic-CMOS Biosensors	Rabia Yazicigil / Boston University
2:30 PM - 3:00 PM	**3097.001**: Reaction Kinetics for the Incineration of Fluorinated Organic Chemicals	Franklin Goldsmith / Brown University
3:00 PM – 3:15 PM	**Break**	
3:15 PM – 4:15 PM	TAB CAUCUS AS NEEDED – TAB MEMBERS ONLY	
4:15	**END OF DAY 5**	

https://www.src.org/calendar/e007869/

Thank You!

Opens?

John Oakley
Science Director
John.Oakley@src.org



Kashyap Yellai
Program Manager
Kashyap.Yellai@src.org

SRC

SRC's Three Pillars for Semiconductors' "Roaring 20s"

Prosperity

Jan 2021

2030 Decadal Plan for Semiconductors

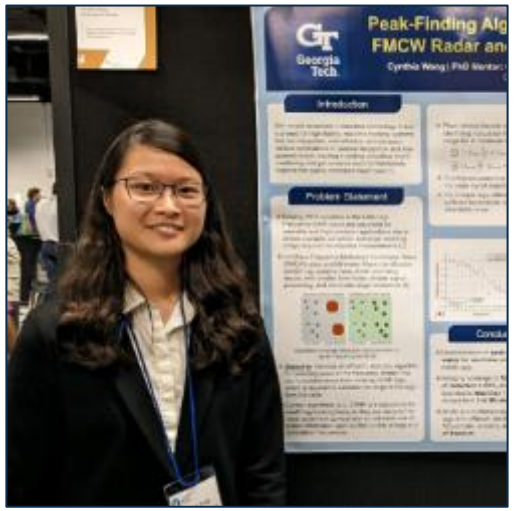
3x↑ in Annual Funding

Oct 2023

Roadmap for Microelectronics and Advanced Packaging (MAPT)

www.src.org/about/nist-mapt-roadmap

The People



Apr 2021

Broadening Participation Pledge

3x↑ Scholar Pipeline (AA-PostDoc)

Greater Diversity, Equity, & Inclusion

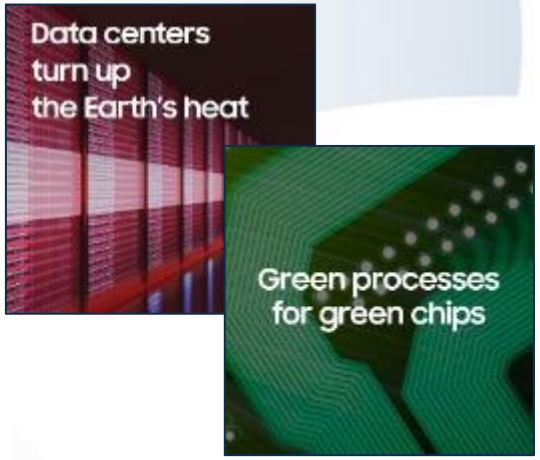
Ignite passion for Semi in US

Workforce Advisory Board (WAB)

www.src.org/about/broadening-participation/

The Planet

Images from Samsung



Oct 2021

Commitment to Sustainability

Green Materials & Processes

Energy Efficient ICT Systems

Win Hearts & Minds of Next Gen Innovators

https://www.src.org/about/sustainability/

Since Spring-2022, SRC has used these 3 criteria to drive all new investments

Guidance for Depositing Supporting Code and Data with Pre-Publications

As part of our move to Pillar Science, there is the ability to collect not just the pre-publications PDF's but also arbitrary file formats (.mp4, .ppt, etc.) as well. This new capability enables a new way for SRC programs to facilitate technology transfer to our sponsors.

Going forward, we will be requiring that all code and supporting data below a certain size threshold to reproduce a pre-publication also be uploaded to Pillar Science.

- SRC's reasons for doing this are:

1. **To more fully document the research output of our programs to demonstrate to our sponsors the breadth and depth of the funded work**
2. The full value of code and data is not often found with its original author but when used across a wider scientific community like our sponsors
3. By having better data and code visibility in our programs, our sponsors will have a better understanding how to connect with researchers

Historically, there has been concern amongst researchers that the code and the data are not "camera ready" for distribution at the pre-publication state. **While these concerns are valid, perfect is the *enemy* of accomplishment.**

- SRC seeks to obtain a snapshot of your code at the state it was in when you submitted your publication to the SRC repository.
- If your code and data are not in a state that you would want to post on an open code repository like GitHub, that is acceptable. Our sponsors employ trained professionals who have the experience to handle and interpret idiosyncratic legacy code and documentation.
- SRC would also like the data collected and used to generate publications to be submitted to Pillar Science as well.
- **Preferably in a single compressed file in an open format marked with the publication's name followed by data so that it read like this, "[Publication Name]_data.ZIP".**

The submission of data to SRC is a direct ask, although it is a right granted by terms of the sponsored research agreement.

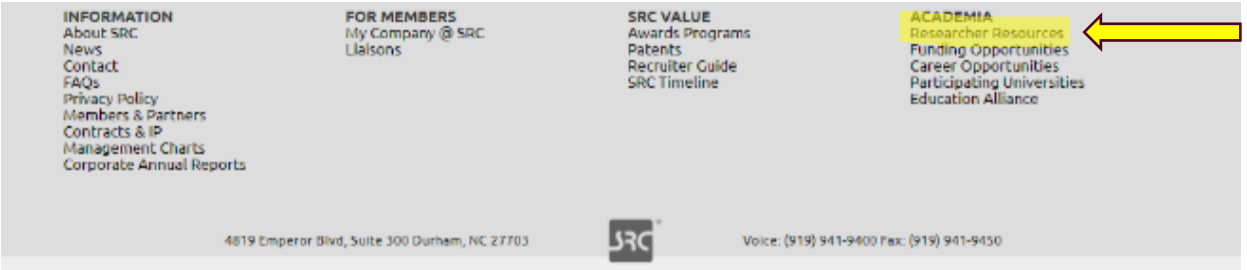
- **Contained within that compressed file should be the data used to generate figures, any code developed for that publication as well as any experimental data acquired if the file size is below 10 Mb.**
- If the data file is in a proprietary file format as often happens with analytical instruments, please convert it to an open format before uploading
- If you are not able to convert from proprietary file format to an open file format, please include it in the compressed data file anyway.
- If the data was acquired from an open depository like the UCI Machine Learning Repository, a notification of that along with a dated weblink in a .txt file should be included.

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/14019093083163-Guidance-for-Submitting-Supporting-Code-and-Data-

Resources that Help Academics Evaluate, Adopt, and Amplify Emerging Member Solutions

Member Resources

- SRC has collected information members provide for the academic community, including education, design, and prototyping
- SRC researchers and students are encouraged to take advantage of these resources in their research and education activities



Member Resources

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Intel

- Intel Open Data Center Diagnostic Project
- Intel Academic Compute Resource Environment (ACE)
- Intel Academic Program for oneAPI

Analog Devices

- Active Learning Program
- ADALM-SR1 Hardware
- ADALM-SR1 Switching Regulator Active Learning Module

ARM

ARM Academic Access
ARM Education

- ARM University Program Education Kits
- ARM Education Online Courses
- ARM Education Textbooks and Reference Books

Texas Instruments
Specific tutorial and curriculum for universities include:

- Texas Instruments University Program
- TI Robotics System Learning Kit
- TI Power Management Lab Kit
- TI Experimental Power Electronics Reference and Curriculum
- TI Precision Labs

IBM

- IBM tutorial and curriculum for universities
- IBM Skills Academy
- IBM + Coursera
- IBM PhD Fellowship Program
- IBM Quantum Computing - student opportunities
- IBM AI Hardware

NXP

- Rapid IoT Prototyping Kit

Siemens

- EDA Academic Products

Qualcomm

- University Relations Program

https://www.src.org/program/grc/guide/researcher/guidelines/

Pillar Science Common Issues & Links for Academics

- There are lots of help articles in Pillar Science which can help answer these questions.

- Here's an article about logging into Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/11198322803099-How-To-Login-to-Pillar-with-SRC-org-Credentials
- Here's an article about update your profile in Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330492961563-How-to-Edit-Your-Profile
- Here's an article about adding students, administrators, or other academics to your project
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330872380187-How-to-add-Students-Admins-or-other-Academics-to-Your-Project
- Here's an article about submitting projects results and deliverables
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/11213311626139-How-to-Submit-Project-Results-previously-known-as-publications-
- SRC hosted a live demonstration for academics on January 31, 2023, and the recording is available
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/12543067480091-Pillar-Science-Demonstration-for-Academics-Video-Recording-

SRC

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/sections/11359770755483-How-Tos-for-Academics

Scholar Expectations

- **Scholar Profile** – Scholars should register for an account on the SRC website, https://www.src.org/app/account/register/step/1/
  - The profile should be maintained in Pillar Science as current as possible.
- **Resume** - Should be uploaded to Pillar and updated as necessary. There are opportunities for internships and full-time hiring from across SRC's members.
- **SRC Scholars program**: Scholars are encouraged to create a LinkedIn account and add "SRC Research Scholars" as experience, https://www.src.org/student-center/handbook/linkedin/ . This is useful to connect with industry and job recruiting opportunities.
- **TECHCON** – All scholars are eligible to submit an abstract. However, Scholars in their second year (or later) of graduate studies are required to submit an abstract to the SRC TECHCON conference per the stated deadline for that calendar year. (Conference held in Sept.)
- **Annual Review** - Scholars are encouraged to present a student poster and co-present with principal investigator.

Pillar Science Common Issues & Links for Industry

- There are lots of help articles in Pillar Science which can help answer these questions.

- Here's an article about logging into Pillar Science
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- Here's an article about update your profile in Pillar Science
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10330492961563-How-to-Edit-Your-Profile
- Here's an article about adding yourself as a liaison
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/10092535189403-How-To-Add-Yourself-As-A-Liaison
- Here's an article about how to find research projects of interest
  - https://semiconductorresearchcorporation.zendesk.com/hc/en-us/articles/9194403647131-Using-Projects-Page
- There was 2 industry demonstrations for industry on February 14 and 21
  - The recordings can be found on the SRC.org website at : https://www.src.org/pillar/

SRC

https://semiconductorresearchcorporation.zendesk.com/hc/en-us/sections/11366772078235-How-Tos-for-Industry

SRC Liaison Program

Maximizing the Value of Participation

Move Yourself, Your Company and the Next Generation Forward

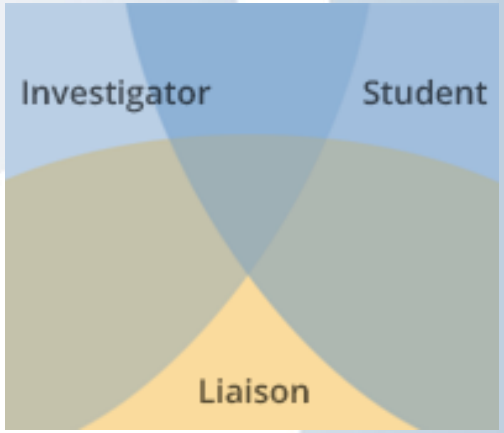
Develop the Workforce

- Provide relevant guidance for industry challenges
- Prepare students to enter industry or pursue future academics

Contribute to Research

- Encourage technology exchange between university and industry
- Bridge the conventional gap between academia and industry

Expectation to have regular PI-Liaisons calls at least one every 4-8 weeks



Academia Contributes to Industry

- Provide an out of the box approach to current problems which enhance industry research and development enables a differentiated product for the marketplace
- Provide an outside perspective adding diversity to the thought process of how best to attack a challenge

Access New Technology

- Gain valuable insights into problems and solutions that will ultimately impact industry competitiveness
- Provide an effective way to deliver actionable research results directly into their companies

Identify the Best

- Identify the most compelling research from current and recent research

SRC

https://www.src.org/liaison/

SRC's Amazing Community

Academics solving meaningful problems
Increase of tech transfer to industry
Clear investment Return Of Investments

SRC Program Manager

- Runs Advisory Board and aligns research
- Educates PI about requirements and responsibilities
- Encourages Liaison participation
- Finds opportunities for further engagement

University Principal Investigator

- Pursues ambitious, ground-breaking research
- Schedules regular calls, every 4-8 weeks
- Arranges meet-ups at conferences
- Presents research at annual reviews

Research Scholar

- Leads meetings
- Presents findings
- Aims to present at TECHCON
- Is knowledgeable about SRC members

Industry Liaison

- Provides industry perspective to PI
- Transfers technology & people into company
- Advocates for SRC research
- Coordinates with Advisory Board

SRC