thinking forward

1999 annual report

Semiconductor
Research
Corporation

photo courtesy of Novellus Systems, Inc.

1999

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The annual report of the Semiconductor Research Corporation is published each year to summarize the directions and results of the SRC research program, present the formal financial report and provide information on activities and events of the SRC community for the previous calendar year.

A copy of this report and additional information about SRC are accessible on the World Wide Web at http://www.src.org.

Looking back

vision

Semiconductor Research Corporation (SRC) will provide competitive advantage to its members as the world's premier research management consortium in delivering relevant research results and relevantly educated technical talent.

mission

SRC's mission is to cost-effectively exceed members' expectations by delivering:

- Managed, innovative, semiconductor technology research responsive to members' needs and guided by the ITRS, focusing on universities
- Relevantly educated university graduates
- Timely transfer of research results
- Strengthened university semiconductor technology capability through partnerships with members
- Collaboration to enhance commercialization and leveraged research.

Photo by Ross Mehan

Erich Bloch Receives the Semiconductor Industry's Highest Honor

robert n. noyce award

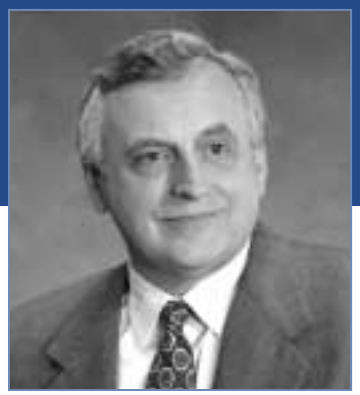
1999 Robert N. Noyce Award –

The Semiconductor Industry Association awarded the industry's highest honor for leadership, the Robert N. Noyce Award, to Erich Bloch (right), founding chairman of SRC. Dr. Dwight Decker (left), Chairman and CEO of Conexant Systems, Inc., presented the award at the SIA's 23rd Annual Forecast and Awards Dinner in San Jose on October 27, 1999. The annual award recognizes individuals for their outstanding achievements in support of the US semiconductor industry.

"The leadership of Erich Bloch in creating an era of cooperation in the semiconductor industry has been an important factor in the continued leadership of this US industry and has established a paradigm for many cooperative undertakings," said Decker. "His vision, character and passion has helped our industry grow and remain competitive in today's world markets."

thinking forward

Message from the President and CEO



Larry W. Sumney

We applaud the SIA's decision to recognize Mr. Bloch with the Noyce Award, and in that spirit, we dedicate this annual report to him.

It is fitting, as we enter the new millennium, that the semiconductor industry has recognized Erich Bloch, SRC's "founding father," with its highest award for leadership. SIA President George Scalise said of the presentation of the Robert N. Noyce Award, "The SIA Board of Directors selected Erich Bloch because of his lifelong contributions to the semiconductor industry and his vision to address technological competitiveness of the industry."

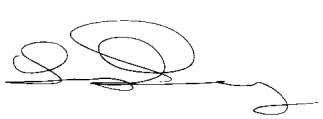
SRC continues to realize Erich Bloch's extraordinary vision by conducting the largest continuous industry-driven university research program in the US. With the support of our members, in 1999 SRC has:

- *Funded $37 million in contracts and grants to 63 universities in the US and Canada;*
- *Provided financial support for 937 students representing technical talent for the industry;*
- *Supported 63 Doctoral fellowships and Master's scholarships;*
- *Rewarded excellence by outstanding teachers and researchers;*
- *Partnered with Novellus, the UMC Group and SpeedFam/IPEC, to create the first "SRC Copper IC Design Challenge;"*
- *Began the detailed planning for our first new topical consortium. Topical consortia enable subsets of SRC-member companies to fund research of particular interest;*
- *Alerted the semiconductor industry to the coming crisis in technical talent through a report documenting the falling number of Electrical Engineering undergraduates;*
- *Co-sponsored with Semiconductor Safety Association and SEMATECH, an award recognizing research excellence in manufacturing and in environment, safety and health (ES&H);*
- *Supported two MARCO Focus Center Research Programs in design/test and interconnect sciences.*

We also have expanded SRC's reach by globalizing our membership criteria and welcoming UMC as our first international member. At the same time we continue to expand our North American membership base.

1999 was an exciting year for SRC. We look forward, with your help, to continuing to honor Erich Bloch's vision of what will be in the new century.

Sincerely,



Larry W. Sumney

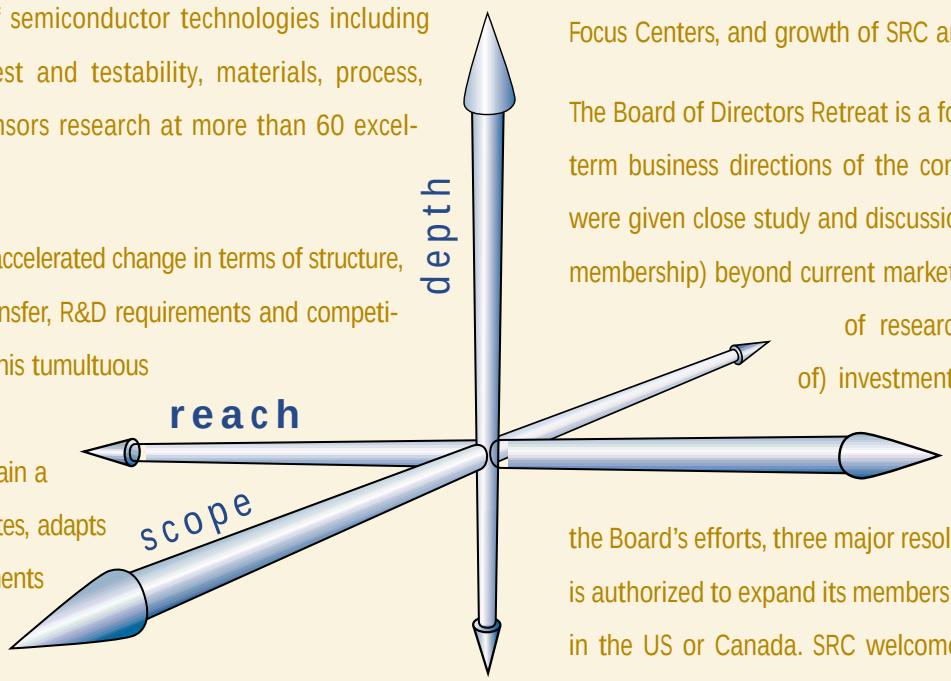
about SRC

Pioneers In Collaborative Research

SRC was established as a not-for-profit consortium in 1982 by leaders of the Semiconductor Industry Association (SIA) to nurture and grow university capability in performing pre-competitive research. These visionary leaders correctly saw the need for using collaborative research as a tool for advancing the pace of R&D for technology development, which in turn drives industry competitiveness. The semiconductor industry has been described in recent years as the engine driving the growth of the larger electronics industry in a time of growth and prosperity. SRC plays a crucial and valued role by contributing to the continuous flow of research results and technical talent for the information age economy.

Over the eighteen years since its inception, the industry has invested more than $520 million in SRC and its participating research organizations. Currently, the research portfolio is targeted to the full spectrum of semiconductor technologies including circuit and system design, design tools, test and testability, materials, process, devices, modeling and simulation. SRC sponsors research at more than 60 excellent universities throughout North America.

The semiconductor industry is characterized by accelerated change in terms of structure, products, applications, markets, technology transfer, R&D requirements and competition. The challenges ahead for the industry in this tumultuous environment imply increasing reliance on collaborative research. The SRC's imperative is to remain a vibrant and dynamic organization that anticipates, adapts and responds to changing technology requirements facing the industry. In order to accomplish this, SRC creates forums for members of its constituency to review and analyze technology trends and set the strategic direction of research investments and value delivery.



Strategic Events In 1999

SRC conducted two strategic events in mid-1999: The ETAB biennial Summer Study and the Board of Directors Retreat. The Summer Study is a forum convened to update and sharpen the SRC's technology investment plans. In 1999, the Summer Study participants examined four key issues; the International Technology Roadmap for Semiconductors and its impact on students, positioning SRC research investments for potentially disruptive technologies, development of needs for the next MARCO Focus Centers, and growth of SRC and its research funding.

The Board of Directors Retreat is a forum for updating the long-term business directions of the consortium. Three dimensions were given close study and discussion: SRC's reach (in terms of membership) beyond current markets and regions, SRC's depth of research programs and (amount of) investments, and scope (breadth of coverage) of research programs. As a result of the Board's efforts, three major resolutions were approved. SRC is authorized to expand its membership to companies not based in the US or Canada. SRC welcomed UMC to membership in January, 2000. SRC was authorized to launch up to three top-

ical consortia which would address the specific needs and interests of subsets of the SRC membership. These topical consortia would provide a mechanism to increase the investment in very focused areas of the research portfolio. The Board created an ad hoc committee to develop a process and forum to formalize the efforts to update the long-term business and strategic direction of the consortium. The Board of Directors Retreat will become an annual event. All of the strategic initiatives are guided by the SRC community's strong focus on maximizing value for the membership and fulfilling SRC's vision of becoming a premier research management organization.

(left to right) Dinesh Mehta, SRC; Peter Chang, UMC; Larry Sumney, SRC and Fu-Tai Liou, UMC.

SRC Welcomes First International Member

Larry Sumney, President & CEO of the Semiconductor Research Corporation, commented, "We welcome UMC as our first international member. We have been working closely with UMC to promote the adoption of copper interconnect technology through SRC sponsored Cu Design Challenge. UMC's position as a global leader in advanced process technology makes them the logical choice for our first overseas member company."

Fu-Tai Liou, senior vice president of UMC, said, "We are very honored to be the first international member of SRC. Our alliance with SRC offers US engineering students the opportunity to come in contact with some of the industry's most advanced technology, including UMC's 0.18 micron copper process. This is a win-win situation for SRC and UMC. Many of these students will go on to join the thriving IC design community currently working with first-tier foundries like UMC to drive innovation in the semiconductor industry."

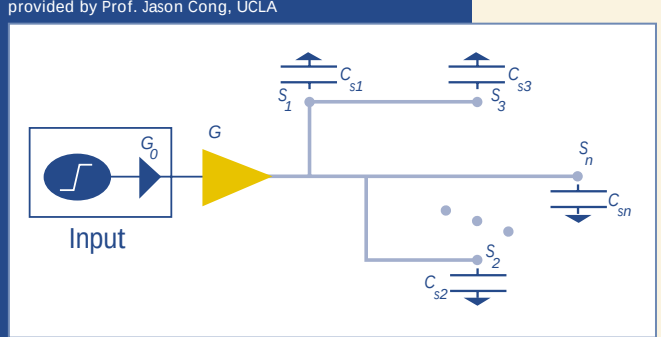
Peter Chang, CEO of Foundry Operations at UMC, offered these comments, "Our admission as the first overseas member of SRC clearly shows that today's technology world recognizes no international barriers. The majority of our partners are US-based design houses, so we feel it is appropriate that UMC use its affiliation with SRC to support the fundamental research required for the continued development of the IC industry."

research contributions

research contributions

SRC operates an integrated research program involving over 200 faculty and over 700 students. Research is conducted in four science areas, each of which is comprised of several research thrusts. The research addresses the complete spectrum of technology needs comprehended by ITRS '99. SRC member company evaluations of the relevance, progress and quality of the research projects reveal a high level of satisfaction with the research portfolio. Herein a few projects are described to provide insight into the productivity and quality of SRC research.

provided by Prof. Jason Cong, UCLA



New efficient performance estimation models predict interconnect behavior at early stages.

CADTS – CAD and Test Sciences

Interconnect Design and Planning – Design methods that account for interconnect technology limitations offer the potential to manage some of the interconnect issues identified by the *1999 International Technology Roadmap for Semiconductors (ITRS)*. Professor Sachin Sapatnekar and his students at the University of Minnesota have developed procedures for interconnect aware global routing with driver size optimization and buffer insertion, and techniques for analysis of crosstalk caused by coupling capacitance. Several member companies have used these methods in tools for IR drop analysis and noise analysis, capabilities that will be a key feature of next generation physical design tools.

Professor Jason Cong at the University of California at Los Angeles has also been making contributions to the interconnect planning area. The efficient and accurate performance estimation models that he and his students have developed predict interconnect behavior at early stages of design (Figure 1). These models have been used to develop wire-sizing strategies for multi-pin nets and to reduce the wire-width assignment problem to selection between a small number of predetermined widths.

Analog Circuit Synthesis – The emphasis on the design of systems-on-a-chip has stimulated an increased focus on mixed signal and analog design automation tools for an area that has been the province of the human designer. Professors Rob Rutenbar and Rick Carley at Carnegie Mellon University, with their students, have produced an analog circuit synthesis strategy and analog synthesis tools in close cooperation with several member companies. Full circuit synthesis of a commercial device produced a design with better noise and area characteristics than one generated by hand.

Verification and Synthesis – Professors Fabio Somenzi, Gary Hachtel and students at the University of Colorado at Boulder, have been working at the forefront of design verification, incorporating formal verification techniques, for several years. Their work, in collaboration with

that at the University of California at Berkeley, is rapidly inserted into synthesis and verification software made available to SRC members and university researchers. In 1999 their guided search techniques, that allow user input to direct automatic checking techniques, gave 60x improvement over previous methods in experimental trials.

Formal verification continued to advance in SRC-supported work, both in terms of the foundational underpinnings and practical use. Professor Thomas Henzinger at the University of California at Berkeley, Professors Randy Bryant and Ed Clarke at Carnegie Mellon University and Professors Allen Emerson and J. Strother Moore at the University of Texas at Austin continue, separately and cooperatively, to make key advances in model checking, processor verification, non-BDD approaches and other techniques. Their tools have shown significant run time improvements and their methods have been incorporated into member company verification efforts.

Test and Testability – Signal integrity problems due to crosstalk are predicted to increase with smaller feature sizes, higher frequencies, reduced noise margins and process variations. Techniques for validating timing using a crosstalk automatic test pattern generation tool and time-based simulation for increasingly larger regions of a circuit have been developed by Professors Melvin Breuer and Sandeep Gupta and their students at the University of Southern California. A new gate delay model captures the effects of transitions at multiple inputs and provides more accuracy than static timing analysis.

Professor Sujit Dey of the University of California at San Diego has developed a suite of design tools addressing increased substrate and power bus noise in deep submicron designs. A simulation framework, including a SPICE-level crosstalk fault simulator, a test generator and a chip-level simulator including behavioral interconnect modeling is available to members.

Thermal Simulation – Temperature-aware simulation techniques are important when analyzing electrostatic discharge (ESD) and when developing SOI technology. Related tasks at the University of Illinois at Urbana-Champaign led by Professors Steve Kang and Elyse Rosenbaum are addressing these important issues and research results are in use by member companies.

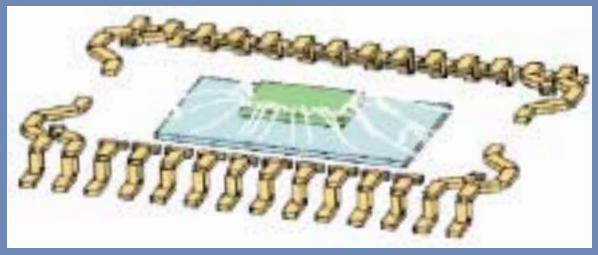
ICSS – Integrated Circuit and Systems Sciences

Interconnect Network Extraction and Synthesis – Accurate and efficient extraction of LC networks is mandatory for high-complexity circuit design. Professor Lawrence Pileggi and his team at CMU have implemented a buffering and sizing approach using higher order delay metrics and have developed a new global clock routing algorithm using the H-Gamma delay metric. They are also developing new methodologies for enabling full system extraction of L (inductance) and C (capacitance) based on simplified approximations. This research has heavy industry interactions with a total of 17 liaisons on the three tasks and, in addition, several students have served as industrial interns.

Synthesis of Ultra-High Speed Random Logic Blocks – Professor Carl Sechen and his team at the University of Washington are using novel approaches to develop the "absolute fastest" digital logic circuits, with clock frequencies in excess of 1 Ghz, by considering completely new families of logic, including Clock Delayed Domino. They have completed a CMOS cell layout generator for arbitrary combinational logic expressions and have demonstrated some phenomenal performance results on standard benchmarks (a side benefit of this logic may be lower power). This project has heavy industry interaction and is important to product development where a standard library of high-speed logic is needed for high performance. Significant advantages may be realized over conventional techniques.

Adaptive Gridding Techniques for Interconnect, Package, and Micromachined Structure Analysis – Tools for fast and accurate RLC analysis are a requirement for high-performance deep sub micron (DSM) IC, IC package, and System-on-Chip designs. Professor Jacob White and his team at MIT have developed new methods for fast and accurate interconnect evaluation for design including a surface-only formulation for distributed RLC analysis which is stable and accurate from DC to light. (Figure 2) They have found a method for model order reduction (Vector-ADI) that is efficient and has good wideband accuracy. Models have been used by member companies for PC board, package and substrate analysis. One company has successfully productized FastHenry and these RLC Analysis techniques. Ten of Professor White's graduates have recently joined industry.

FIG. 2 provided by Prof. Jacob White, MIT



Adaptive Gridding techniques for high frequency package analysis.

High-Speed High-SFDR Converter Design – Professor Ramesh Harjani and his students at the University of Minnesota are developing a high-speed, spurious free, dynamic range data converter for digital wireless basestations (50+Ms/s at 16 bit with ~100db SFDR). The team reviewed various architectures to identify components that limit linearity and has derived analytic expressions for nonlinearity of the input sample-and-hold block. This work has given member companies additional insight regarding architectural tradeoffs.

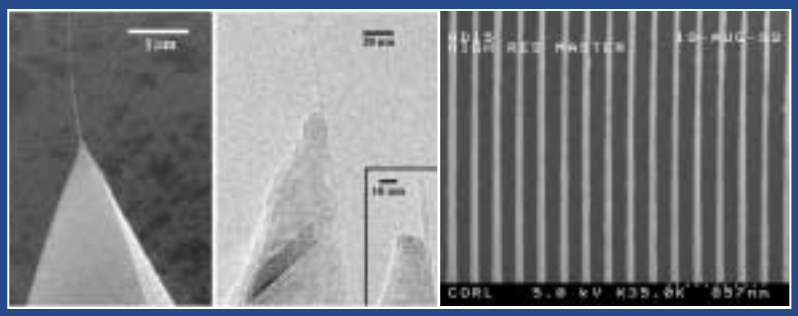
MPS – Material and Process Sciences

Patterning

Advanced Resist Research – Professor Grant Willson, University of Texas-Austin, was awarded SRC's 1999 Aristotle Award for his contributions to the education of students in the art of resist design, synthesis and characterization. This team discovered a new and general mechanism for resist dissolution. This molecular level model of polymer dissolution promises to serve as a basis for lithography simulators that use fundamental materials properties, rather than empirical fits to experimental data. These results help to enable optical lithography through at least the 70 nm technology generation.

Maskless Patterning – A multi-university team from Stanford (Professors Pease, Quate and Dai), UC-Berkeley (Oldham and Frechet), UT-Austin (Willson) and MIT (Smith) have collaborated to demonstrate the feasibility of several novel, potentially disruptive, maskless patterning options, such as AFM, dendrimer-based resist carbon nanotube arrays, and step and flash patterning (Figure 3). These results provide a quantitative understanding of the capabilities and limitations of the known approaches to maskless lithography and demonstrates the capability, including patterned wafers and working devices for several promising technologies and may also identify new approaches to maskless lithography.

A B



Examples of a) single nanotubes grown on AFM tips and b) 60 nm features patterned via Step and Flash Patterning

FIG. 3

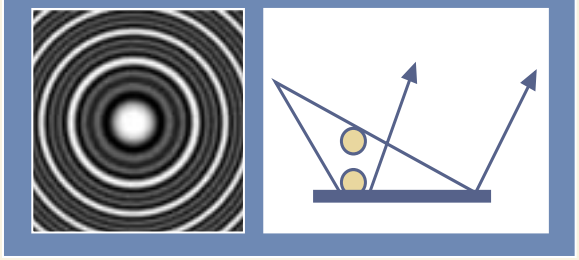
a) provided by Prof. Hongjie Dai, Stanford
b) provided by Prof. Grant Willson, UT/Austin

Patterning Metrology

Point Projection Microscopy – Professor David Joy and his students at the University of Tennessee at Knoxville were awarded SRC's 1999 Technical Excellence Award for research on Advanced Techniques for E-Beam Metrology and Lithography, emphasizing nanoscale feature metrology options. This effort created a new noninvasive approach to dimensional metrology using coherent electron beams (Figure 4). This powerful nondestructive technique for measuring critical dimensions of 3D nanoscale structures is critically needed to extend IC manufacturing below 100nm.

provided by Prof. David Joy, Univ. of Tennessee

FIG. 4



Hologram resolves two 5nm spheres 5nm apart one above the other using 50eV coherent ebeam.

Wavefront Engineering – Professor Jeff Bokor's team at the University of California at Berkeley is developing metrology necessary for characterizing wavefront aberrations in short wavelength lithography optics at the operational (actinic) wavelength from 193 nm down to 10 nm. The metrology methods developed under this project are being used by the EUV Consortium and serve to guide the design and characterization of EUV related optics.

Environment, Safety and Health

Benign Materials Research – Professor Christopher Ober's and Professor Karen Gleason's team at MIT deposited and imaged a novel dielectric thin film resistless and solventless patterning process, during the first year of support. This research demonstrated the feasibility of resistless and solventless patterning materials and processes that eliminate wet chemistry during the thin film deposition and image development steps (Figure 5). Potential benefits include reduced manufacturing costs due to process integration and a reduction in the numbers of unit processes and competitive high-performance and benign patterning materials and processes. This endeavor is supported by the joint SRC/NSF Engineering Research Center (ERC) in Environmentally Benign Semiconductor Manufacturing. It is part of a multi-university initiative from MIT and ASU (Professor Raupp) that explores sustainable and environmentally benign photolithography, deposition and etch materials, and processes in semiconductor manufacturing.

FIG. 5

provided by Prof. Christopher Ober, Cornell Univ. and Prof. Karen Gleason, MIT

1um and 500 nm lines patterned using resistless and solventless lithography from joint SRC/NSF ERC in Environmentally Benign Semiconductor Manufacturing.

Front-End Processes

High Permitivity Gate Dielectrics – As the MOS transistor continues to scale, better gate dielectrics are needed to obtain required transistor drive while maintaining sufficient voltage breakdown levels and low-leakage currents needed for low power designs. Two SRC research projects have made contributions to developing high permitivity gate dielectrics applicable in the equivalent oxide thickness (EOT) regime of 1 nm. Professor Stephen

FIG. 6

provided by Prof. Stephen Campbell, Univ. of Minnesota

Campbell of the University of Minnesota has demonstrated high permitivity films at about 1 nm EOT (Figure 6). In addition, Professor Dim-Lee Kwong and his students at the University of Texas at Austin have demonstrated a high permitivity gate dielectric with an equivalent oxide thickness of less than 1 nm. This is a significant milestone because of the need for an appropriate interfacial layer and the necessity for careful thickness control. A tantalum pentoxide-nitroxide gate stack structure having an EOT of 9.86 Å was demonstrated. The sample's interfacial barrier layer was formed by NH_3 passivation, and it was annealed in both hydrogen and oxygen after Ta_2O_3 deposition. A TiN/aluminum metal gate was used.

Modeling of Ion Implantation – Professor Al Tasch and his students at the University of Texas at Austin have developed and implemented a convolution/deconvolution capability in UT-MARLOWE, an ion implantation modeling code, that can account for the collisional broadening effect observed in SIMS measurements of impurity profiles in ultra-low energy ion implants. They have also developed the ion implant models (electronic stopping and nuclear scattering) for Ge and In implants in single-crystal and amorphous Si. They have completed the first phase of a computationally efficient cumulative damage (dose dependent) model for high B and P implants, and made significant progress in developing models in UT-MARLOWE for 2-D and 3-D profiles of implants through topographically varying surfaces and through multiple layers.

Mechanisms of Dopant Diffusion – At Stanford University, Professor Jim Plummer and his team have made significant advances in elucidating the doping issues in <0.1 um MOS devices. They conducted experiments that shed light on the effects of concentration on boron-interstitial cluster formation, diffusion and activation. Additional experiments determined the fractional contributions of microscopic diffusion mechanisms for common dopants and self-diffusion in Si. They directly observed that arsenic pile-up forms a monolayer on the Si side of the Si/SiO_2 interface and that the monolayer is easily incorporated into the native oxide when the Si surface is exposed. The researchers also demonstrated the important role of Solid Phase Epitaxy in dose loss for low energy As implants. Although the basic mechanisms for dopant diffusion (used extensively in front end processing) in silicon are well established, many unanswered questions still remain. Contributions include increased understanding and modeling for **1**) the role of surfaces and interfaces on dopant loss and segregation, **2**) Transient Enhanced Diffusion (TED) mechanisms when low implant energies are used, and **3**) dopant diffusion and activation/deactivation at very high concentrations.

New Defect Detection System – At Arizona State University, Professor Dan Hirleman (now at Purdue University) and his team invented a new hybrid (photon-electron) defect detection system. They have developed the framework that established far UV or EUV scattering and e-beam scattering as the most likely candi-

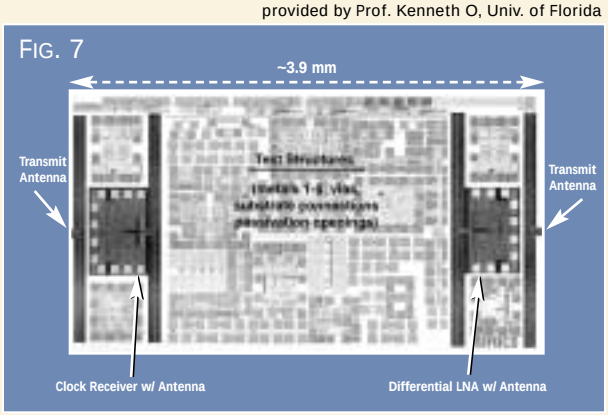
dates for ~20 nm particle detection. The researchers conducted both experimental and theoretical work on EUV scattering by particles. This research not only concluded that a pure EUV approach should not be pursued, but also led to the invention and recommendation of a novel hybrid (photon-electron) technique.

Back-End Processes

New thinking required to solve the upcoming Interconnect problems – At the 0.1um technology node and beyond IC Chip areas are expected to exceed 1000 (25X40) mm^2, and on-chip clock frequencies are expected to be above 2GHz. At these geometries and speeds the conventional metal-dielectric interconnects cannot provide the needed high speed connectivity among many critical circuit elements, e.g. for global clock distribution needs. Professor Ken O and his students at the University of Florida are exploring a radical alternative to conventional metal-dielectric interconnect- the use of wireless transmission using microwaves (Figure 7).

provided by Prof. Kenneth O, Univ. of Florida

FIG. 7



The system envisioned could be realized completely on a single chip, with transmitters and receivers at ends of the clock lines. Alternatively, a multichip system might transmit clock signals to multiple receivers. Professor O and his students have demonstrated many of the components of this system, as well as verifying the system viability from the standpoint of noise and power. In these efforts they have designed, fabricated, and evaluated linear, zigzag and dipole antennas, designed inductors with Q factors greater than 20 at 20 GHz, and designed, fabricated and characterized transmitter and receiver circuits in 100 nm technology.

NIS – Nanostructure and Integration Sciences

Advanced Devices and Technologies

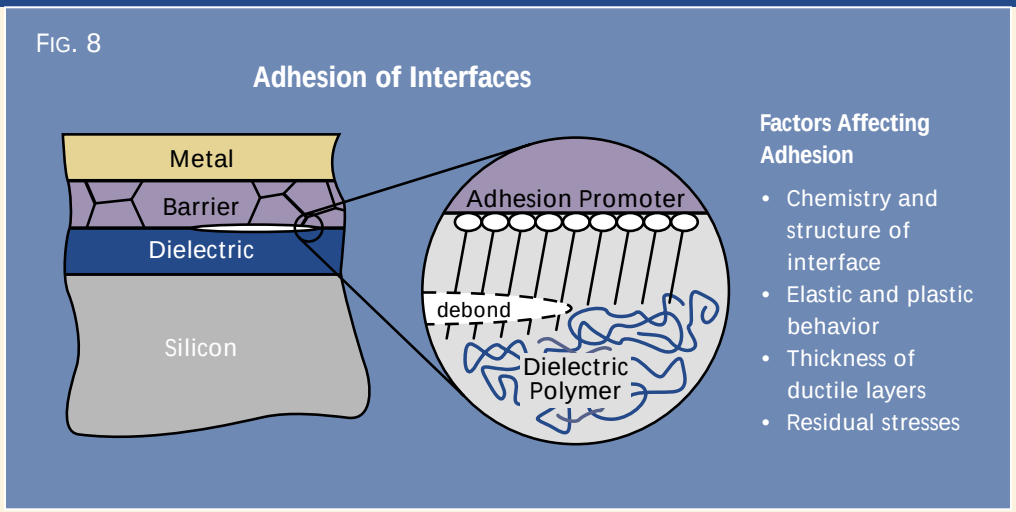
Compact MOSFET Modeling Using BSIM – Professor Chenming Hu's team at the University of California at Berkeley has substantially extended the BSIM Compact Model BSIM4 to comprehend demanding new requirements. These new requirements include predictive capability for future process generations, accurately modeling RF device performance and inclusion of new physics related to sub-100-nm MOSFETs. BSIM4, for the first time, contains the physics necessary to model RF devices. New parameters modeled include gate and substrate resistances, noise partition effects, transit-time dependent non-quasi-static effects, pocket and retrograde dopant profiles, multi-finger device structures and an improved 1/f flicker noise model. BSIM4 is now available to SRC members as a beta test version for evaluation.

Packaging and Interconnect

Interface effects and mechanical failure of IC packages – Bi-material couples that occur with increasing frequency in IC packaging applications typically possess widely different physical and mechanical properties (e.g., coefficient of thermal expansion, thermal conductivity, elastic modulus, fracture toughness and strength). These different material properties inevitability lead to significant residual stresses in the package that, in turn, provide the driving force for interface delamination and failure.

Professors John Bravman and Reiner Dauskardt, along with their students at Stanford University, have made fundamental contributions to correlating surface chemistry interactions with mechanical performance of interfaces. They have studied the resistance to de-bonding of the Silicon/Oxide/BCB (Benzocyclobutene) system interfaces. This interface system is

FIG. 8



provided by Profs. John Bravman and Reiner Dauskardt, Stanford Univ.

prevalent in many IC multilevel metal and packaging systems. A study of the effects of the curing temperature of the silane coupling agent on mechanical failure modes has isolated a mechanism responsible for failure. In particular, this study has shown that samples cured at 90 degrees centigrade de-bond via cohesive failure of the BCB film, whereas for those cured at 75 degrees centigrade the crack propagates through the adhesion promoter layer. Study of the chemical-mechanical system shows that the lower curing temperature causes insufficient cross-linking of the silane chain molecules and as a result the interface is substantially weaker compared to the samples cured at 90 degrees centigrade. (Figure 8)

Semiconductor Modeling and Simulation

Dopant Profile Extraction Technique for Sub-100-nm MOSFET Characterization – Professor Dimitri Antoniadis and his students at MIT have pioneered a potentially accurate and efficient method for extracting 2-D dopant profiles from subthreshold leakage currents for deep submicron MOSFETs. A new inverse modeling technique will potentially provide an accurate method for obtaining the required 2-D dopant distributions. Their technique is based upon determining doping profiles for which simulated electrical characteristics match experimental data. The experimental techniques chosen are such that the electrical properties exhibit strong dependence on the dopant distribution. Current-voltage data in the weak inversion region (i.e., subthreshold current) are quite sensitive to non-uniform doping and to short channel effects. Additional work is underway to fully demonstrate the utility of this technique (e.g., to confirm the uniqueness of the solutions for dopant profiles).

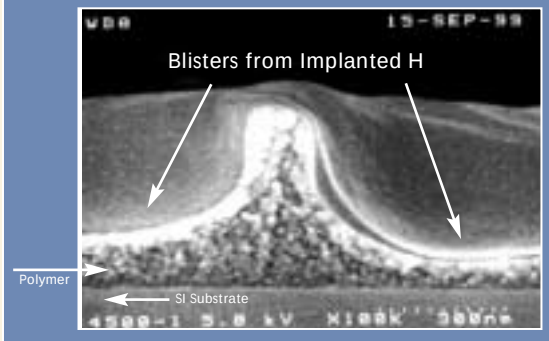
Sub-100-nm MOSFET Benchmark Models – "Well-Tempered" (i.e. well behaved) sub-100-nm MOSFETs should continue to operate in an essentially classical (i.e. non-quantum) manner for some time as scaling continues. A variety of MOSFET modeling and simulation tools have been developed and applied to simulation of sub-100-nm MOSFET structures. These tools include Drift-Diffusion, Hydrodynamic and Monte Carlo modeling techniques. The typical tradeoffs of validity/accuracy versus speed of analysis traditionally differentiate the applicability of these simulation tools to particular sub-100-nm MOSFET structures. A recent workshop on "Nanotransistors: Technology, Physics, and Simulation," organized by Professor Mark Lundstrom of Purdue University and others, called for a set of standard, well-behaved sub-100-nm MOSFET structures to be created and made available to the device modeling and simulation community for benchmarking new simulation tools. Professor Dimitri Antoniadis of MIT, in response to this need, designed, simulated and, in one case (90-nm), fabricated and characterized 90-nm, 50-nm and 25-nm MOSFET structures. He has made available to the simulation community experimental (90-nm) and simulation (50- and 25-nm) results for benchmarking and comparing the various simulation tools.

CSR – Cross-disciplinary Science Research

In 1999, SRC began a research program to encourage unconventional thinking among university faculty and students on topics that may offer a potential solution for the myriad of technical challenges facing the industry. The program was structured to encourage cross-disciplinary research and to enable the participation of faculty from non-traditional disciplines. Seventy-seven innovative concept papers were received from the university community, and ultimately, ten of these concept papers were funded via a grant for an exploratory phase. SRC anticipates that several of the funded projects will result in a proposal to one of SRC Science Areas for further research.

provided by Prof. Cindy Desmond-Colinge, California State Univ./Sacramento

FIG. 9



New efficient performance estimation models predict interconnect behavior at early stages.

The funded projects include quantum dot cellular automata, a silicon-based quantum computer, quantum mechanical simulations for fullerene-based molecular electronics, nanoscale silicon ultra-high density memory, fabrication of novel 3D structures using silicon wafer bonding (Figures 9 and 10), assembly of optical/photonic circuits, directed self-assembly of interconnect networks for semiconductor devices, VLSI-scale monolithic diffractive optical interconnects, statistical interconnect prediction algorithms, and design, characterization and modeling of self-assembled imageable materials for sub-100 nm lithography.

SRC believes that the CSR program provides an additional mechanism to identify potential technology discontinuities and thereby to influence SRC research program strategic directions.

"...the semiconductor industry is entering domains where traditional assumptions no longer apply and where extraordinary innovation is needed. In a very real sense, the industry will need to reinvent itself over the next decade. We feel that the opportunity to invent at the granularity of matter is a challenge worthy of our best minds..."

Ralph K. Cavin III, SRC

quoted in Stanford's Spring, 1999, CIS Newsletter

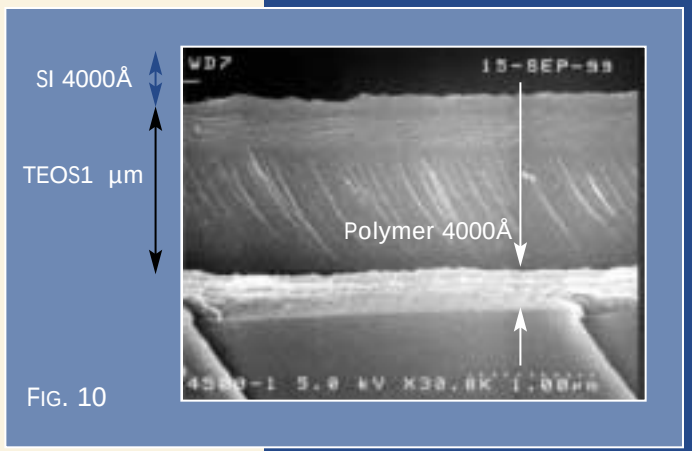


FIG. 10

Transfer of 4000Å Si layer with deposited TEOS using hydrogen splitting

provided by Prof. Cindy Desmond-Colinge, California State Univ./Sacramento

copper design contest

SRC's Copper Design Contest

In 1999, SRC in conjunction with Novellus Systems, Inc., UMC and SpeedFam/IPEC, launched the SRC Copper Design Challenge, a contest intended to spark interest in novel circuit designs that exploit demonstrating the power of novel use of copper interconnects. The contest offers over $150,000 in cash prizes and $850,000 in technical services and design implementation and support. The contest is being conducted in two phases and is scheduled to come to completion in 2000, with the phase two winners to be announced at TECHCON 2000 in Phoenix in September 2000.

SRC Cu Design Challenge
NOVELLUS • UMC GROUP
SpeedFam-IPEC

The contest's objective is to create novel circuit designs that will help accelerate the adoption of copper technology by engaging the creative interest of university faculty and students. These new designs are intended to exploit the capabilities offered by advanced semiconductor processes using copper. Specifically, contestants are designing a circuits or circuit subsystems (clock network, analog building block, etc.) that utilize the enhanced properties of the copper interconnect technology to achieve significant functional or performance gains over the same circuits constructed from traditional aluminum interconnect technology. The contest sponsors are looking for creativity, unanticipated innovations, and the very best usage of the emerging technology. Phase one will determine which contestants have offered the most promising designs and have the opportunity to have their designs fabricated by the UMC's world class foundry.

The response to the contest has been very encouraging to SRC, Novellus, UMC and SpeedFam/IPEC, with 44 teams from 34 universities answering the call for entries. The entries received by SRC focused on five technology areas; interconnect architecture, digital implementation, mixed-signal implementation, technology/component and wireless/RF. The participating universities are listed below, by category:

Participating Universities

(By Entry Category)

Interconnect Architecture

Carnegie Mellon University
Georgia Institute of Technology
Michigan State University
Oregon State University
The City College of the City University of New York
The State University of New York at Buffalo
University of Illinois, Urbana-Champaign
University of California, San Diego
University of Florida
University of South Florida
Yale University

Digital Implementation

Carnegie Mellon University
North Carolina State University
North Dakota State University
University of California, Los Angeles
University of Illinois, Urbana-Champaign
University of Massachusetts, Amherst
University of Southern California
University of Utah

Mixed-Signal Implementation

Duke University
Purdue University
University of Colorado
Virginia Polytechnic Institute and State University

Technology/Component

Boston University
Carnegie Mellon University
Illinois Institute of Technology
North Carolina State University
Oregon State University
Rensselaer Polytechnic Institute
University of Minnesota
University of Virginia

Wireless/RF

Arizona State University
Carnegie Mellon University
George Washington University
Kansas State University
Ohio State University
Rice University
The City College of the City University of New York
University of Washington
Washington State University

src web site

SRC Web Site

Targeted as the key mechanism for delivering value in information, the SRC Web site saw substantial growth in 1999 in both content and usage. With over 17,000 pages of content and 3,000 active users, SRC has clearly established a prominent and successful value delivery mechanism by integrating a comprehensive base of information about the SRC research program into the daily information workflow of personnel that contribute to and gain value from it.

The secret behind SRC's highly successful Web site is a strong conviction that to deliver value SRC must first proactively identify, embody and manage value. Simply stated, this required the establishment of robust and highly efficient support processes tightly coupled with critical information management technologies to ensure the quality, reliability and timely delivery of all aspects of SRC's research program and operations.

While the SRC Web site and all supporting processes and technologies have continued to evolve since its initial inception in 1996, several significant new capabilities were brought online in 1999:

Growth in content: The shear volume of content of information on the site grew by nearly 50% this year. While much of this increase can be attributed to the ongoing nature of SRC's research portfolio, the growth was also a result of integrating new content areas. For example, 1999 saw the integration of all new research solicitations coupled with the posting of all white papers and proposals for subsequent review.

Growth in the user base: SRC saw nearly a 50% increase in the number of active users in 1999. This resulted in part due to a 1999 effort to better serve and support the needs of our researchers via the SRC Web site.

Better targeting of information: Whether intended for a subcommittee of an advisory board or the SRC Board of Directors, much new information was placed on the site in a secured manner and targeted for specific subsets of the user community. SRC's Web delivery strategy is directed towards those users who can best contribute to and benefit from it.

Going beyond simple information delivery: While success of the SRC Web site has in large part been due to rapid access to a wealth of information, the site has been further expanded to promote interactivity and simplify processes that were previously paper or email based. For example, an Industrial Liaison application form is now one click away from each and every task description in the SRC research catalog.

Push technology implemented: Early in 1999, SRC implemented the ability for any user to establish a profile of interests that formed the basis for initiating a monthly "push" of email to a user to promote awareness of what's new at SRC in the user's chosen areas of interest. The email provides a brief description of the new content, such as new SRC events or highlights stemming from a particular research effort, combined with a direct link to more in-depth information to be found on the SRC site.

As with all aspects of the World Wide Web, SRC cannot rest on its laurels. The coming year will once again see substantial improvements on the site with a strong focus on promoting collaboration and streamlining the bi-directional flow of information.

www.src.org

student programs

An Investment In Students

937 students participated in SRC-funded research in 1999, up from 874 in 1997. Of that 937, 145 graduated with the Ph.D. or Master's degree as compared to 178 in 1997 and 153 in 1998. Students performing their doctoral or master's research under SRC-funded contracts provide an excellent source of technology transfer through internships and permanent hire. Increasing numbers of SRC graduates are building the links between the membership and SRC by serving as Technical Advisory Board Members, Industrial Liaisons, and even one Board of Directors member. Research tasks with former SRC students are also increasing as they join existing contracts or submit their own proposals. The SRC community is seeing an outstanding return on its investment in students – an investment well worth preserving.

The Graduate Fellowship Program Annual Conference

The 1999 Graduate Fellowship Program Annual Conference was held in Austin, Texas, September 13-14, 1999. Ten invited student papers and 41 posters were presented. Outstanding Research Presentation awards went to Dennis Sylvester and Bassam Tabbara both from the University of California at Berkeley. The keynote address was given by Dr. Robert Dennard, IBM Fellow; corporate sponsorship was provided by AMD and IBM. Attendance at this conference was over 100 including Board Members, Technical Advisory Board Members, Industry Advisors and GFP Alums, as well as the Graduate Fellows and Master's Scholars.

Human Resource Needs Roadmap Project

A study of human resource needs for the semiconductor industry into the twenty-first century was completed and a proposal was presented to the SIA and SRC Boards of Directors in October of 1999. SRC Board approved SRC management of the University/Engineers segment of the proposed programs; the SIA Board approved implementation of three undergraduate programs at the University/Engineers level and one at the K-12 level to be managed through the SIA. These programs are scheduled to be implemented, beginning in 2000 as funding is identified.

Bassam Tabbara, SRC Graduate Fellow at UC-Berkeley, receives an award from Dr. Dinesh Mehta for "Outstanding Research Presentation" at the 1999 GFP Annual Conference.

Other Highlights

- 52 Fellowships were supported under the Graduate Fellowship Program. Of the 8 Fellows completing the GFP in 1999, 5 joined member companies or university faculties.
- 16 Company-Named Fellowships were in place during 1999 as follows: AMD, 3; IBM, 2; Intersil, 1; Motorola, 4; National Semiconductor, 2; Texas Instruments, 3; NIST, 1.
- The first Research Fellowships were put into place by Hewlett-Packard and AMD.
- 11 Master's Scholarships were supported under the Master's Scholarship Program. Of the five Scholars completing the program, 3 are pursuing the Ph.D. (one as an SRC Fellow) and 2 have joined SRC member companies.
- Of the 145 graduates, 55% went to work for SRC member companies, 20% joined university faculties and 6% were undergraduates who are continuing their education.

photo by Roger Winstead, North Carolina State University

graduate fellowship

The Graduate Fellowship Program

The Graduate Fellowship Program (GFP), created in 1986, addresses the issues of improving educational opportunities at the doctoral level and supplying a relevantly educated work force for the semiconductor industry. The GFP is designed to attract exceptionally talented students with US/Canadian citizenship or permanent resident status in the US to academic areas of interest to SRC members. While Fellows are not required to take employment within the SRC community, they are strongly encouraged to do so, and assistance is provided in finding appropriate employment.

Graduate Fellow Jeff Snodgrass, Stanford University, and Master's Scholar Adreane Kelly, Lehigh University, were among the students at the 1999 Graduate Fellowship Annual Conference who used the event to share research results to build networks.

Graduating Fellows entering SRC member companies facilitate the transfer of new science and technology from the participating universities to the supporting organizations. Fellows joining faculties at US/Canadian universities carry with them the expertise to stimulate new research activities and to encourage additional student interest in semiconductor-related fields.

GFP Fellows

Andrew Abo
University of California/Berkeley

Peter Abramowitz
University of Texas/Austin

Michael Beattie
Texas Instruments/SRC Fellow
Carnegie Mellon University

Michael Booth
Cornell University

Christopher Borst
Rensselaer Polytechnic Institute

Arthur Bradley
Auburn University

Heidi Cao
University of Wisconsin/Madison

Danny Chen
Cornell University

Jir-Shyr Chen
IBM/SRC Fellow
Cornell University

Karen Coperich
National Semiconductor/SRC Fellow
University of Illinois/ Urbana-Champaign

Joel Fenner
Robert M. Burger Fellow
North Carolina State University

Brian Floyd
Intersil/SRC Fellow
University of Florida

David Fryer
Texas Instruments/SRC Fellow
University of Wisconsin/Madison

Glenn Glass
Motorola/SRC Fellow
University of Illinois/ Urbana-Champaign

Heidi Gundlach
State University of New York/Albany

Stefan Hau-Riege
Massachusetts Institute of Technology

Noel Hoilien
University of Minnesota

Gregg Hoyer
University of Washington

Anna Ison
Motorola/SRC Fellow
University of California/Berkeley

Maura Jenkins
Stanford University

Simon Karecki
Motorola/SRC Fellow
Massachusetts Institute of Technology

Norman Kay
University of Arizona

Jean Kelsey
State University of New York/Albany

Michael Krasnicki
Carnegie Mellon University

Jing-Rebecca Li
Hewlett-Packard Research Fellow
Massachusetts Institute of Technology

Aaron Lilak
University of Florida

Francisco Machuca
Stanford University

Derek Martin
University of Florida

Clayton McDonald
Advanced Micro Devices/SRC Fellow
Carnegie Mellon University

George McMurray
University of California/Berkeley

James O'Keeffe
Stanford University

Michael Orshansky
Advanced Micro Devices/SRC Fellow
University of California/Berkeley

Shipra Panda
National Semiconductor/SRC Fellow
Carnegie Mellon University

Michael Perkins
Stanford University

Thomas Pistor
University of California/Berkeley

Igor Polishchuk
NIST/SRC Fellow
University of California/Berkeley

Laura Pruette
Motorola/SRC Fellow
Massachusetts Institute of Technology

Sriram Rajamani
University of California/Berkeley

Benjamen Rathsack
Texas Instruments/SRC Fellow
University of Texas/Austin

Lance Robertson
IBM/SRC Fellow
University of Florida

Brad Shutzberg
Cornell University

Jeffrey Snodgrass
Stanford University

Michael Stewart
Advanced Micro Devices
Research Fellow
University of Texas/Austin

Robert Sumners
Advanced Micro Devices/SRC Fellow
University of Texas/Austin

Dennis Sylvester
University of California/Berkeley

Bassam Tabbara
University of California/Berkeley

Nerissa Taylor
University of Illinois/ Urbana-Champaign

Robert Thacker
University of Utah

Shawn Thomas
University of California/Los Angeles

Andy Wei
Massachusetts Institute of Technology

Chad Weintraub
North Carolina State Univeresity

Xin Yi Zhang
Stanford University

Master's Scholars

Paul Ampadu
University of Washington

Cassondra Crotty
Purdue University

Andres Gutierrez
University of Florida

Adreanne Kelly
Lehigh University

Jamie Ludke
University of Arizona

Francisco Machuca
Stanford University

Toussaint Myricks
University of Washington

Adrian Robinson
Rensselaer Polytechnic Institute

Tamara Tubbs
Georgia Institute of Technology

Enrique Velasco
GEM/SRC Scholar
Stanford University

Jaimal Williamson
Georgia Institute of Technology

aristotle awards

Photo courtesy of Toland Sand Glass Studio and Light Opera Gallery

The Aristotle Awards

The Aristotle Award was created by the SRC Board of Directors in March 1995 to recognize faculty whose deep commitment to the educational experience has had a profound and continuing impact on SRC students and their professional performance. This Award is intended to acknowledge outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project.

Two Aristotle Awards were presented in 1999 recognizing excellence in teaching through the research process. The awards were presented at the Graduate Fellowship Program Annual Conference in Austin, Texas to Professors Roxann Engestad and Grant Willson.

Aristotle Award Winners

Professor Engelstad is associated with SRC-funded research through the Center for Nanotechnology at the University of Wisconsin-Madison. Her students speak of her ability to balance student interests with industry needs, facilitating important, sustained and lasting contributions to industry. Her students have multiple opportunities to leave school before completing their degree, but the importance of completing the degree is so well understood that not one of her students has been enticed to leave without the degree. She is an excellent role model for her students; her enthusiasm, technical understanding, and clarity of thought and expression are key to her exceptional performance as a teacher.

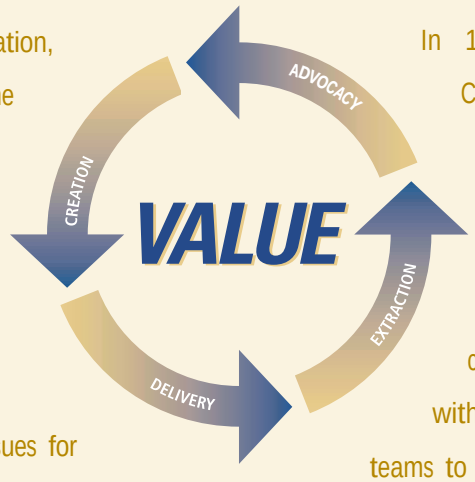
Professor Willson is the Rashid Engineering Regents Chair and Professor of Chemistry and Chemical Engineering at the University of Texas-Austin. His students report a total commitment to insuring that the students under his supervision gain a broad range of experiences and are exposed to a variety of challenges. He has the ability to "excite students and draw them into the process of invention and discovery." He is a strong proponent of involving undergraduates in research. Professor Willson's former students are making significant contributions to the SRC community, and many are involved in SRC research as Industrial Liaisons.

value management

SRC's Value

SRC's members consider four key outputs (products) as providing value to the membership. These are Research Results, which respond to the difficult challenges articulated in the ITRS; Technical Talent, graduates who are the future scientists and engineers so critically needed for the continued growth of the industry; Integrated University Research Capability, developed through SRC sponsorship of university research over the past eighteen years; and Networking Opportunities, that SRC facilitates throughout the management of SRC programs and events.

SRC's value proposition focuses on all dimensions of value including the creation, delivery, extraction, and advocacy (including communication) of value for the benefit of all members. In order to remain vibrant and strong, the SRC community (members, university faculty and students, government and SRC staff) works together to continuously revitalize the products, processes, programs, tools and systems necessary to fulfill its consortia purposes.



Team Accomplishments

The annual member survey was significantly improved to identify key issues for focused attention. At the survey development stage, focus groups helped refine the survey instruments. The OCE participated in one-on-one interviews to get real time information on member needs and concerns.

A pilot process was initiated to promote technology transfer with SEMATECH and third parties. Built into the methodologies is a model for transferring software that acknowledges the fact that software may be in evaluation stage, ready for limited use internally by members, or ready for commercialization by third parties.

The new, Web-based Industrial Liaison sign up process was established along with an annual audit for updating participation received high marks from SRC members for ease of use and utility. SRC's Web site is the primary delivery mechanism for research results, member services and interaction resources.

Value Managament For Member Satisfaction

In 1999 the Value Chain and Member Communication/ Satisfaction functions were combined to emphasize the interrelation and importance of value delivery, support, service and communication to achieve member satisfaction. The Value Chain TAB continued to serve as an advisory body, within which the members have formed three teams to provide specific guidance in the areas of process effectiveness, communications and industrial liaisons/student interactions. The latter team works jointly with the Student Relations TAB.

Plans For 2000 And Beyond

2000 is filled with promise and opportunities to increase the value delivered to SRC members. As the membership and operations go global, SRC will be modifying the value chain processes to insure that our global members have timely input and access to planning documents, research results and students.

industrial liaison

Industrial Liaison Program

SRC Industrial Liaison Program was launched in 1983 (formerly known as the Mentor Program) to provide a formal framework for human interactions that stimulate creativity and solve technical challenges. The role of the Industrial Liaison has grown and evolved over the years. Today Industrial Liaisons fill three distinct roles: Facilitators, who provide information and material support to advance the progress of the research; Mentors, who guide and encourage those students aspiring to enter the semiconductor industry; Advocates, who ensure that knowledge and research results are returned to their company and brought into use.

Each year SRC recognizes individuals who have made significant contributions as Industrial Liaisons. This year, the awards have been re-named in honor of one individual whose commitment and dedication to the Industrial Liaison Program served as a role model for others. Dr. Mahboob Khan, of AMD, built from scratch one of the best managed and most successful mentor/liaison programs of any SRC member company. He shared his model and ideas with other companies and advocated for a strong, ongoing commitment to research and support of the individual liaisons. He held leadership positions on several advisory boards over the years and took an active role in assuring that SRC provided consistent value to its members. Dr. Khan passed away on April 16, 1999. In recognition of Dr. Khan's contributions to the industry, to SRC, and to the liaison program, henceforth these annual awards will be known as "The Mahboob Khan Mentor Awards."

This year, two individuals were recognized for their unselfish contributions to both industry and academia. Their work reflects breadth and imagination and has had a lasting effect on the larger community.

Mani Janakiram, Intel Corporation — In 1997, SRC mounted a major new initiative in Factory Sciences that posed considerable challenges for forging an effective partnership among SRC, the National Science Foundation, and three competing teams of university researchers. Mani Janakiram stepped up and took charge of this difficult project. In his role as Industrial Liaison, he described an overall vision for the proposed work, opened and developed lines of communication among the research teams and industry, and worked closely with selected graduate students. He worked tirelessly to bring the benefits of these interactions back to his company through workshops, recruiting additional liaisons, and encouraging participation of his company's fabs in the research process.

James Ryan, IBM Corporation — For more than seven years, James Ryan has been involved with the research program at the State University of New York at Albany and Rensselaer Polytechnic Institute. Whether he is mentoring or advising undergraduate or graduate students at the University, leading and/or serving on various Master's and Doctoral thesis committees, or counseling the many university faculty and students who constantly seek him out, Dr. Ryan is doing what he does best: being an inspiring counselor, effective tutor, and exemplary citizen of the SRC community. James Ryan regularly presents specialized courses, technical presentations, and training seminars to both students and faculty at the university. He has provided valuable and relevant summer internships to a number of students, and has recruited a significant number of graduates for IBM.

technical excellence

Technical Excellence Awards
Recognizing Research That Accelerates Innovation

Since its inception in 1991, SRC's Technical Excellence Award has recognized 50 researchers and 16 major research efforts whose technological contributions have significantly enhanced the productivity of the US semiconductor industry. Each year a research team is chosen based on the team's creativity and innovation, scientific merit of their research, value to industry of the results and effectiveness of the team at technology transfer.

The 1998 Technical Excellence Award was presented to Professor Sung-Mo (Steve) Kang of the University of Illinois at Urbana-Champaign for his work in "Modeling, Simulation and Design Guidelines for VLSI Reliability," and to Professor David Joy of the University of Tennessee for his work in the area of "Ultra-Low Energy Electronic Imaging for Metrology at 0.13 and Below."

Sung-Mo (Steve) Kang, University of Illinois at Urbana-Champaign

Dr. Kang's research is in the area of modeling, simulation and design guidelines for VLSI circuit reliability, particularly to assure the immunity of a circuit's input/output (I/O) buffers to electrostatic discharge (ESD) and electrical overstress (EOS). These effects are significant reliability problems, since continued technology scaling makes it harder to protect integrated circuits from ESD/EOS damage. The insights and computer-aided design (CAD) tools provided by Dr. Kang's research guide engineers in designing I/Os for emerging technology generations that are immune to ESD/EOS.

Dr. Kang introduced the Power Profile Technique as an effective method to assess the EOS/ESD reliability of integrated circuit pins.

David Joy, University of Tennessee at Knoxville

Dr. Joy was honored for his research in metrology, specifically in the areas of characterization and measurement. His laboratory at the University of Tennessee is developing new techniques in the fields of Transmission Electron Microscopy (TEM), Scanning Electron Microscopy (SEM), Scanning Tunneling and Atomic Force Microscopy, confocal optical microscopy, and in related methods of energy dispersive X-ray spectroscopy (EDXS) and electron loss spectroscopy (EELS). He is revolutionizing the understanding of the charging phenomenon and is exploring the use of ultra-low voltage secondary e-beam spectroscopy as a tool for characterizing submicron particles. He is also working on new areas, including the use of holography to permit three-dimensional nondestructive visualization of complex nanoscale structures.

intellectual property

The value of SRC membership is enhanced and protected by providing intellectual property assets spanning numerous SRC-sponsored university research programs. Intellectual property (IP) assets exist to support the SRC's mission and charter to transfer and commercialize the results of SRC-sponsored research programs to SRC member companies. SRC's significant portfolio of IP assets serves to minimize the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use and commercialize the results of research programs funded through SRC sponsorship. IP assets are interwoven with the SRC research catalog and complement the value chain as an important benefit of SRC membership.

In return for sponsorship, SRC receives non-exclusive, worldwide, royalty-free IP licenses in research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background IP licenses necessary to practice SRC research results is provided, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to protect members – by ensuring that those utilizing SRC-sponsored technologies do so only within the scope of a valid license.

US Patents Issued in 1999

Title	Inventor(s)	Filing Date Issue Date	US Patent Number	University
Multi-layered Attenuated Phase Shift Mask and a Method for Making the Mask	Bruce Smith	Mar. 9, 1998 Aug. 17, 1999	5,939,227	RIT
Electrostatically-actuated Structures for Fluid Property Measurements and Related Methods	Raj Gupta Stephen Senturia	Jan. 13, 1998 Sep. 21, 1999	5,955,659	MIT
Oxidation Resistant High Conductivity Copper Layers for Microelectronic Applications and Process of Making Same	William Lanford Peijun Ding	Apr. 22, 1997 Sep. 28, 1999	5,959,358	SUNY/ Albany
Bipolar Transistor Having Base Region With Coupled Delta Layers	Kang Wang Timothy Carns Xinyu Zheng	Sep. 15, 1994 Oct. 12, 1999	5,965,931	UCLA
Silicon-on-insulator transistors having improved current characteristics and reduced electrostatic discharge susceptibility	Chenming Hu Mansun Chan Hsing-Jen Wann Ping Ko Keung	Jun. 5, 1995 Nov. 9, 1999	5,982,003	UC/ Berkeley

During 1999, five SRC-sponsored US patents were issued, bringing the total US portfolio of SRC patents to 161. The patents relate to materials and processes, novel device structures and devices, copper interconnect technology and silicon-on-insulator (SOI) devices. In addition, several SRC-sponsored foreign patents issued. SRC's significant patent portfolio supports both US and international member company operations in numerous countries around the world.

In addition, SRC provides over 170 software programs, software models, and technical databases to member companies. Software and database IP licenses from SRC-sponsored research programs represents a growing and complementary IP portfolio. Members are directed to the online software directory at URL http://www.src.org for further details. SRC members similarly receive licenses in applicable software research outputs.

Marco

MARCO Focus Center Research Program Called "Collaborative Revolution"

"We have initiated the collaborative revolution," said Richard Newton, director of the Design and Test Focus Center at UC/Berkeley, during the center's first annual review. "Through collaboration, we have made a conscious effort to 'lift our heads up' and emphasize long-range vision."

Berkeley and Georgia Tech Collaborate with Others

During their first year, both the UC/Berkeley center and the Georgia Tech Interconnect Sciences Focus Center forged innovative new research relationships with multiple universities, across the boundaries of campuses and science areas. The initial results were promising.

At UC/Berkeley, progress was made toward platform-based design that enables rapid, reliable development of new, specific applications. Some research areas reporting progress in 1999 included component/communications-based design, common standards, constructive fabrics, highly programmable systems and metrics for continuous improvement.

For example, the potential benefits to tools research and development, said Newton, include a methodology for continuous tracking of data over the entire lifecycle of instrument tools, more efficient analysis of realistic data, facilities identifications of key design metrics, effect on tools and improvement of benchmarking. Details of the UC/Berkeley-led research can be found on the web at www.gigascale.org.

Transcending Limits

"Our overarching goal is to transcend the known limits of interconnects that would otherwise decelerate or halt the historical rate of progress," reported James Meindl, director of the Interconnect Focus Center at Georgia Tech.

Six universities are working together, with the leadership of Georgia Tech, to study seven broad areas: system architecture and circuit innovations; physical design tools; novel communications mechanisms; chip-to module interconnects; materials and processing; process modeling, simulation and technology assessment; and reliability and characterization.

"Maybe we can announce, in the next year or so, some entry-level functions using optics," said L.C. Kemerling of MIT, "and put ourselves in the designers' case book."

More details on the interconnect research program can be found at www.ifc.gatech .org.

Commitment to Independent Thoughts

In a feedback session on the first year's results, Sonny Maynard, co-executive director of MARCO said, "Part of the essence of the focus center program, up front, is a commitment to make time for independent thoughts that a room full of industry people might vote down."

1999 proved that the chip industry is committed to new ideas. In fact, industry representatives recommended that the focus centers "move a bit further out in time and technologies." And the Focus Center Research Program Governing Board, on recommendation of the SIA Technology Strategy Committee, the SEMI-SEMATECH (now Semiconductor Industry Suppliers Association) Focus Center Advisory Committee and DARPA, approved the additional topics for two new focus centers to be planned during 2000: Materials, Structures and Devices, and Circuits, Systems and Software. In their first year of operation, the focus centers were clearly up and running.

1999

Members

Advanced Micro Devices
Compaq Computer
Eastman Kodak
Hewlett-Packard
(including Agilent Technologies)
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Intel
Intersil *(formerly Harris Semiconductor)*
LSI Logic
Lucent Technologies
Motorola
National Semiconductor
Northrop Grumman
Texas Instruments
UMC

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Etec Systems, Inc.
Mentor Graphics Corporation
Novellus Systems, Inc.
Shipley Company
Synopsys
Ultratech Stepper

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