Semiconductor Research Corporation

1989 Annual Report

Cooperative Research

The Semiconductor Research Corporation

The Semiconductor Research Corporation (SRC) is an organization of U.S. corporations and government agencies that provides a mechanism for cooperation in support of their semiconductor research and educational objectives. Motivated by the belief that a cooperative program is more effective and productive than independent efforts and by the critical need for augmentation of the technology base in this important technology sector, these organizations have established and supported a broad, university-based research program in semiconductor technology that has become an essential component of the national effort.

Semiconductor devices are the performance enablers for almost all of the electronic products that now account for more than five percent of the U.S. Gross National Product. Rapid advances in all electronics sectors — including consumer and business applications, computers, communications, and aeronautical, astronautical, and defense systems — have been fueled for the last three decades by semiconductor products. The industries supplying these products will comprise the largest share of the future national economy. More than any other technology, semiconductors will determine the competitive success of U.S. industry and, thus, the quality-of-life available to its citizens.

The most important semiconductor product is the ubiquitous integrated circuit. Continuing advances in integrated circuits are foreseen by SRC goals for the year 2001. By that year, a world semiconductor market of greater than $100 billion is forecast,

Cooperative research in the SRC's agenda ranges from integrated circuit and system design to fabrication processes and tools, with heavy emphasis on research related to devices, materials, and phenomena. Some of the research is relatively short range, aiding in the solution of current problems, while other projects address 21st century device concepts. This research is produced by more than 800 university faculty and students, with a comparable number of industry scientists and engineers working with or benefiting from the several hundred distinct investigations being funded. The SRC's 1989 budget for these efforts is about $30 million, most of which was provided by the industrial membership. Government agencies also participate in and provide funding for SRC's research.

The description of research results and other measures of accomplishment during the past year that are provided in this report can only partially represent the impacts of the SRC. Its effects and products reach far beyond the community of participants and are helping in many ways to strengthen the technology base of this country. However, much more remains and must be accomplished to reverse the trends foretelling a weakened technology stature for the U.S. in the future.

SRC
COOPERATIVE RESEARCH

Executive Message

Challenges for the SRC

Mr. Sumney

We could, in this brief message, address the past and take pleasure in the products and accomplishments that have resulted in the SRC's being one of the most successful among cooperative organizations. Rather than doing that, we believe a better message is to focus on those things which have not been done.

The SRC must be challenged to enlarge the footprint of its cooperative research effort on the technology of this industry, to abet the efforts of others in facing and solving the problems associated with US. industrial competitiveness in the semiconductor sector, and to continue to provide a clear advantage to its membership. More specifically, the SRC will direct its efforts to:

- Doing a better job of communicating its activities to the technical community of this country.
- Obtaining the means to focus more completely on a fuller range of silicon device structures and applications, instead of limiting itself to basic integrated circuit technology.

- Building a stronger relationship with its membership at the upper-management level so that the SRC is pushed to expand its organizational role as vigorously as it is being pushed at the research-program level. Innovation and growth must be more strongly encouraged from the top.
- Cooperating more with other organizations with which it interfaces. Strongerties are required among all of the organizations addressing needs of the industry if the maximum benefits are to be obtained from the efforts of all of these organizations.
- Enhancing its technology leadership through the improved planning and integration of its research and through more productive interaction with the research performers.
- Continuing to avoid inefficiencies in its operations and the accumulation of unproductive activities that become common in maturing organizations.
- Continuing to provide the essential correlation of industry needs with the capabilities of universities,

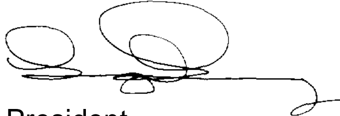
Our vision for the SRC is to build on our success in establishing a relevant and productive semiconductor research program and in addressing other significant needs; to create an organization and activity with a value to the U.S. industry five times that of the present SRC, and with five times the impact. All of us participating in the SRC must contribute to the achievement of this vision. It can be done. We need to do it.

Mr. McMillin

Robert J. McMillin

Chairman of the Board

Larry W. Sumney

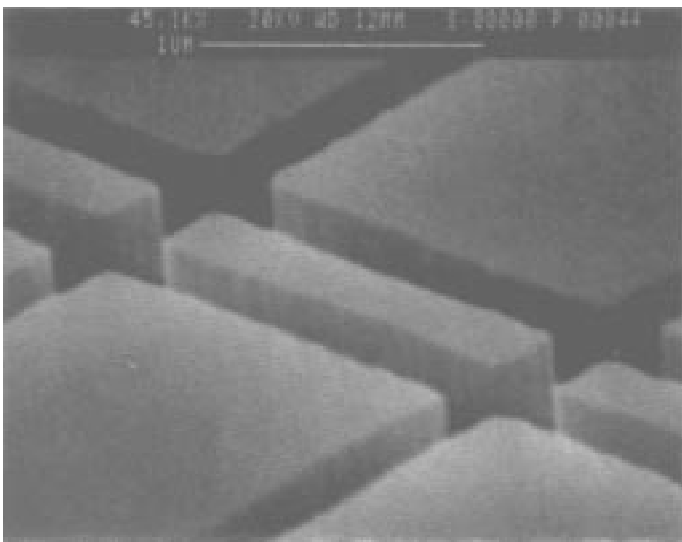


President

SRC
COOPERATIVE RESEARCH

Philosophy of the SRC

The SRC's Research Agenda



Micrograph of a 200-nm-wide etched trench around 300-nm-wide active nanoMOS device area from research led by Professor J.P. Krusius at Cornell University to explore the significance of the extrinsic series resistance of CMOS devices to source/drain sizes in the nanoelectronic domain.

Since the SRC's Research Program is carried out by the academic community, it must be designed with knowledge of the strengths and limitations of such an environment. Universities provide excellent opportunities for cross-fertilization among disciplines: a highly motivated work force of excellent researchers, e.g. graduate students; productive networking with others in the same research area; and an emphasis on exploration and creativity. Since much university research support from other sources consists of grants, an advantage accrues to organizations such as the SRC that define research needs, set goals, and provide strong interactions with the users of the results for practical industry applications. University research is limited by its integration with educational objectives in which the graduate students are part-time researchers and have finite productive tenures, by the tendency of faculty members to be independent, and by the inadequacy of equipment and facilities.

The challenge undertaken by the SRC is to take advantage of the strengths of the universities in defining specific research directed to meeting the needs of the industry that it serves, It must continually seek researchers who have the skills and motivation to respond to the defined needs and must focus strongly on building constructive and efficient interactions with the chosen research performers. That the SRC has done this well is without question, but the challenge to do better must continue to drive its efforts.

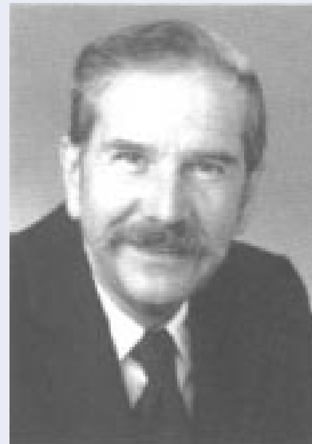
The SRC's research agenda emphasizes silicon integrated circuits because the technology needs in this area were an important factor in the founding of this cooperative organization. Research support from the government had been (and continues to be) focused on compound semiconductor devices, with the result that research relating to silicon devices was very small relative to its industrial importance before the SRC's research mission was initiated. The SRC has restored

an active and productive silicon-device-related research program in U.S. universities and provides most of the support that ensures its continued viability.

Much of the SRC's research is focused on the challenges presented by forthcoming generations of new devices that will require improved lithography tools, a cleaner production environment, design tools with much-improved capabilities, and advances in other microelectronics technologies. The primary objective of research is to create new knowledge that addresses these types of problems in addition to the less-well-defined new concepts for products and processes of the future. Rather than focusing exclusively on improving current products, researchers must have the willingness to explore technologies whose applications are elusive but from which new products will be created.

Research and education are the key functions of the SRC. Some participants attach equal or greater value to the fostering of cooperative relationships among the members for the exchange of viewpoints and information on precompetitive technologies and common concerns faced by the US. industry. All participants — industry, government, and university — benefit from these exchanges within the SRC "community" and are bringing about a much-needed acceptance of cooperation as a way of life for U.S. semiconductor technology.

The SRC's educational activities — fellowships and curricula development — are being transferred to a newly established sister organization, the SRC Competitiveness Foundation. The Foundation is empowered to receive tax-free gifts and to address a broad range of educational needs that relate to high technology.



Mr. Charles E. Sporck
President and CEO,
National Semiconductor Corporation

"The SRC is an outstanding example of how individual competing companies can work together to address important common needs. The SRC has shown us that a carefully planned consortia with a clearly defined mission can work, and that it can contribute significant benefits to all of its members. To me, this was a telling factor in our willingness later on to create SEMATECH.

"When you look at the history of our industry, you can see that the SRC is an outstanding success that must be emulated in many industries it this country is to meet its competitive challenges."

COOPERATIVE RESEARCH

Impact of the SRC

The Strength of the Generic Research Link

Progress for the semiconductor industry can be described in terms of a technology chain in which each link consists of an activity essential to the creation of new products. Research lies at one end of the chain and the production of competitive products is at the other end. Through the U.S. semiconductor industry's cooperative, the SRC, the generic research link in this technology chain has now become strong, thereby meeting the prime goal set for the SRC by its founders.

Competition requires that all links in the technology chain be strong. The SRC, by fostering a strategic plan and initiating cooperative responses in other areas, has recognized that high quality research is not the only requirement for meeting the competitive challenge and is responding. However, research and manpower remain its prime concerns.

Although, the major impacts of the SRC are related to its success in restoring the broad semiconductor research base of the U.S. industry, certain of its impacts have extended beyond research. Without the SRC, the following would not have occurred when they did:

In the Microstructure Sciences:

- the re-establishment of silicon bipolar device research in U.S. universities.
- the continuation of process modeling research that is of great importance to the industry.
- the introduction of new device-related concepts such as post-shrink silicon devices and *in-situ* processing.

Dr. Robert N. Noyce
President and CEO.
SEMATECH

"When we formed the SRC back in 1982, we had high hopes for its success, and we have not been disappointed. The SRC has shown that, by pooling our resources in a cooperative effort, we can get good results that benefit all participants In SEMATECH, itself, one of our first and best decisions was to ask the SRC to manage our university research projects. This is a logical extension of the SRC's activities, and it is already paying big dividends. We have confidence that the university research program is being well managed and that the results of the research will directly contribute to meeting SEMATECH's goals."

In the Design Sciences:

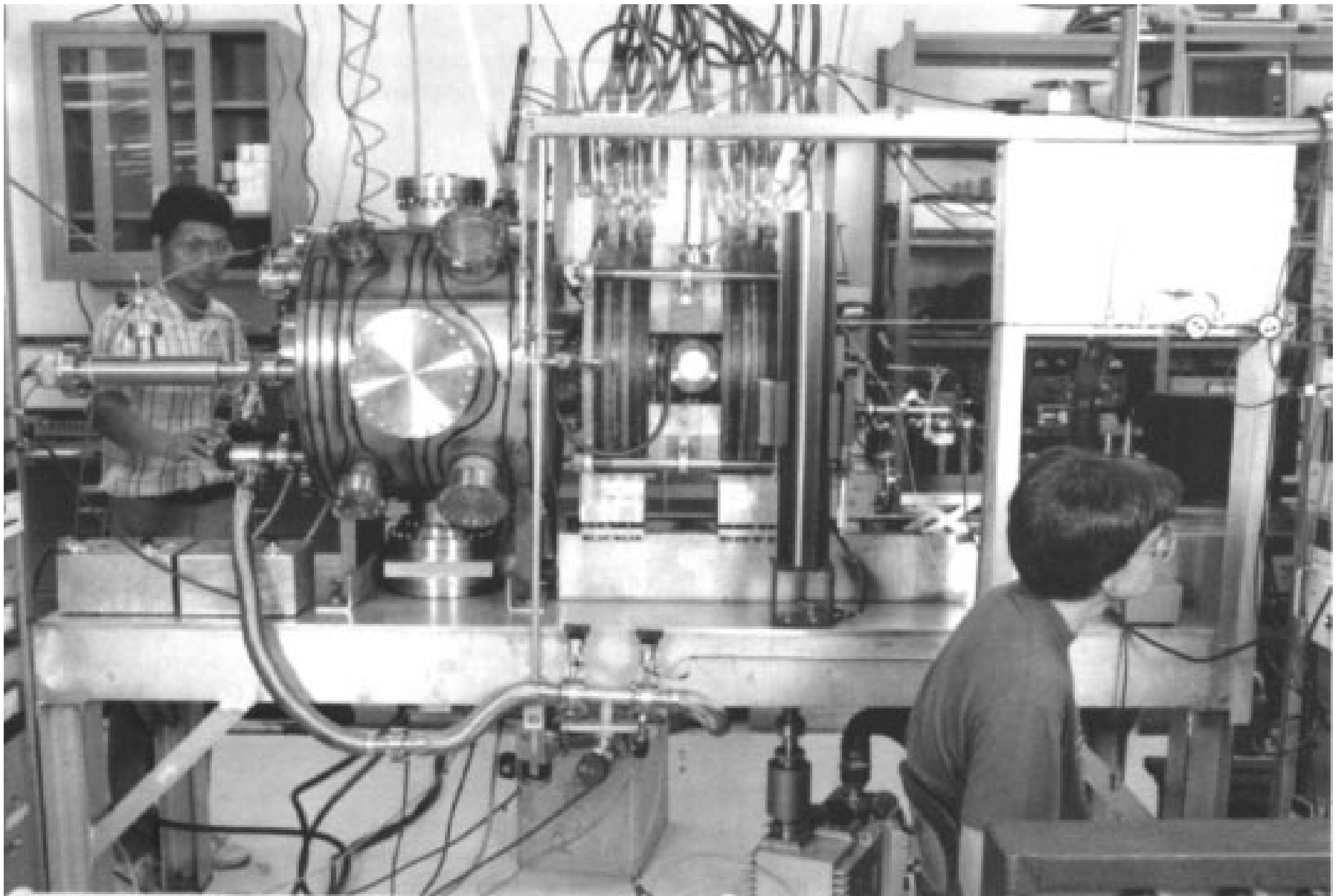
- the nurturing of the strongest design research program in the world.
- the definition of new research directions for the U.S. design research community that ensures its continued preeminence.

In the Manufacturing Sciences:

- the creation and acceptance of new important academic research areas relevant to semiconductor manufacturing.
- the development of curricula for educational programs in semiconductor manufacturing.
- pioneering research to establish equipment models required for semiconductor factory automation.

In the overall SRC Research Program:

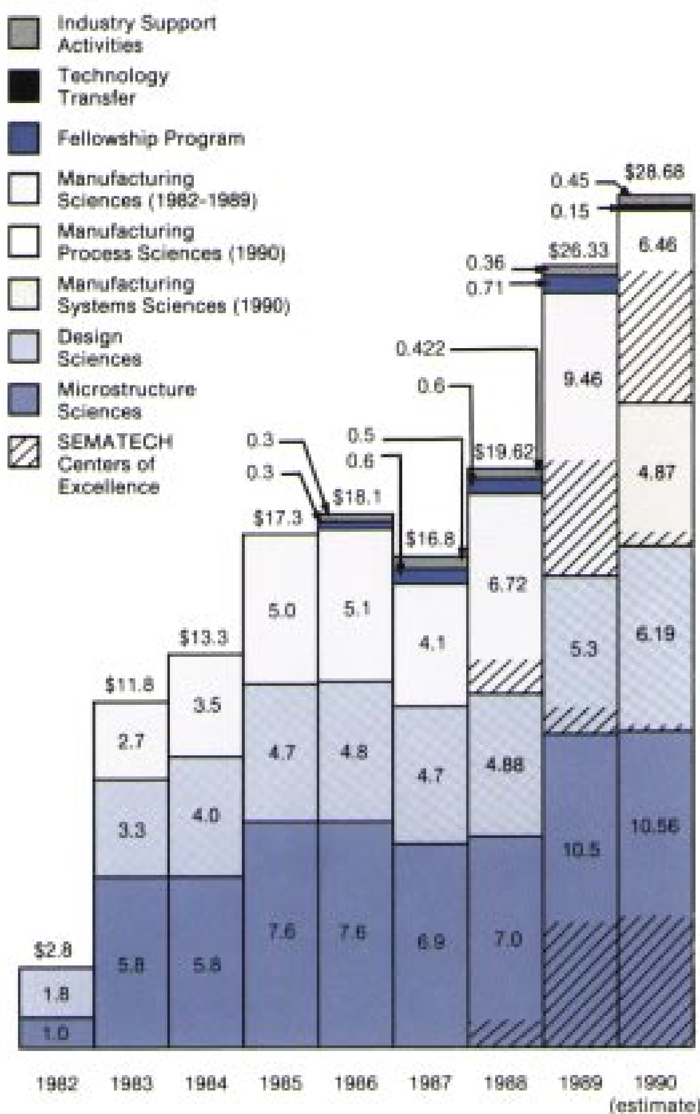
- a dramatic expansion of cooperation in the U.S. through SEMATECH, the National Advisory Committee on Semiconductors, strategy, and government participation.
- A greater than 10-fold increase of M.S./Ph.D. graduates with silicon technology backgrounds.
- increased industry-university interaction through a program in which more than 800 university faculty and graduate students participate in SRC research that is reviewed and/or translated to practical applications by hundreds of industry representatives.



The ECR etch tool at Princeton University

SRC Research Overview

Research Program Commitments
($ in Millions)



Scope of the Research Program

The SRC Research Program is goal oriented. Specific research goals are used to guide, focus, and prioritize research efforts and to provide a basis for measuring progress. The SRC Technical Advisory Board developed ten-year goals in 1984 that state the anticipated industrial member capabilities in 1994. The research of the SRC is directed to make it possible not only to achieve these goals but to accelerate integrated circuit technology development by a two-year period within the ten-year scope of the projections. These goals are referred to as the 1994 goals, and were reassessed this year to confirm their validity and provide the base for extending the goals to 2001.

A major effort was expended in 1989 in identifying the new technology goals in the year 2001. In addition to the technology “push” assessment based on an extrapolation of past technology trends, product “pull” forecasts — focusing on workstations, supercomputers and automotive/industrial needs — were also made to determine if market requirements would accelerate or alter past trends. Discontinuities and, more importantly, the need for creating discontinuities were identified and will be used in 1990 to prioritize the research program.

Science Areas and Goals

The SRC Research Program is partitioned into three “Science” areas: Design, Manufacturing, and Microstructure. SRC research goals are divided into two parts: Global goals, which drive the integrated effort of the overall SRC Research Program, and the goals specific to the Design, Manufacturing, and Microstructure Sciences research areas. Design Sciences addresses new computer tools, systems and methodologies applicable to the design of ICs. Manufacturing Sciences encompasses yield and reliability enhancement, computer integrated manufacturing, packaging,

and manufacturing processes. Microstructure Sciences focuses on device and interconnect structures, new and improved processes, advanced devices, materials and equipment, and mathematical modeling of new processes and devices.

Research Thrusts

Delineating the research into separate science areas does not adequately serve many of the higher-level SRC goals; quite often the exploration of knowledge cuts across defined technical areas, demanding contributions from more than one group. To clearly identify the fields of common study, the SRC has adopted a second interdiscliplinary classification of research called “Thrusts.” The seven operational thrust areas are: Advanced Devices and Device Concepts, Computer-Aided Design, Education, Manufacturing Systems Integration, Packaging, Process Technology, and Reliability.

Roadmaps have been developed by industry representatives to refine and interpret the overall SRC research goals for the selection of specific research thrust areas and individual research tasks.

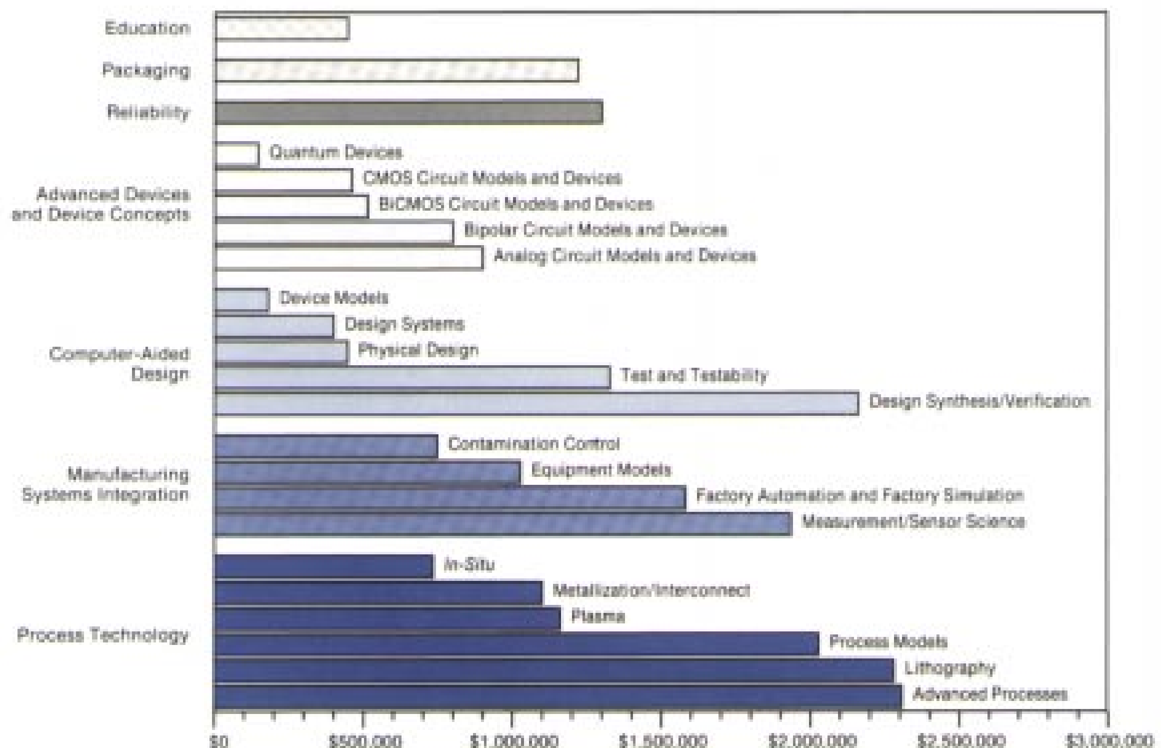
Global Goals

The MC’s global objectives are to attain a:

- 250-fold increase in functionality,
- 104 increase in performance as measured in gate-Hz/cm^2,
- chip reliability of no more than 10 failures in 1 billion hours (10 FITS) with burn-in, and
- 500-fold reduction in cost/functional element;

With full consideration of the:

- capital equipment cost per unit area of silicon processed,
- wafer throughput and process automation,
- disposability of reaction products,
- contamination and defect introduction,
- stability of process results,
- safety of operations, and
- a capability for processing large diameter wafers.



Program Structure

SRC research has three funding-level designations: Center-of-Excellence, Program, and Project.

SRC CENTERS OF EXCELLENCE are funded by the SRC at a level which is typically $1 million to $2 million per year and support 25 to 75 graduate students and faculty. The SRC's Center-of-Excellence designation recognizes an institution's sustained and distinguished record of significant contribution to the integrated circuits field over a number of years, The five SRC Centers are:

- Carnegie-Mellon University for Computer-Aided Design.
- University of California at Berkeley for CAD/IC Design.
- Cornell University for Microscience and Technology.
- University of Michigan for Automation in Semiconductor Manufacturing.
- Stanford University for Manufacturing Sciences and Technology for VLSI.

SEMATECH CENTERS OF EXCELLENCE (SCOE) are research efforts initiated and funded by SEMATECH and managed on behalf of SEMATECH by the SRC. The objective of the SCOEs is to achieve the understanding that will allow development of a competitive manufacturing system designed to meet the challenges of a rapidly changing technology. The focus of SCOE research must remain consistent with the SRC goal set while meeting the challenge of the SEMATECH manufacturing objective. The SEMATECH Centers are designated by State and involve the staff and facilities of several participating institutions. Nine SCOEs were established in 1988 and two additional ones were initiated in 1989. They are:

- Arizona SCOE: Contamination/Defect Assessment and Control
- California SCOE: Lithography and Pattern Transfer
- Florida SCOE: Predictive BiCMOS Process Design for Manufacturing
- Massachusetts SCOE: Single-Wafer Processing for Flexible IC Manufacturing
- New Jersey SCOE: Plasma Etching
- New Mexico SCOE: On-Line Analysis and Metrology for Semiconductor Manufacturing
- New York SCOE: Multilevel Interconnect Systems
- North Carolina SCOE: Automated Microelectronics Manufacturing
  Pennsylvania SCOE: Rapid Yield Learning
- Texas SCOE: Understanding and Modeling of Unit Processes
- Wisconsin SCOE: X-Ray Lithography

An SRC PROGRAM normally supports 15 to 40 researchers, is funded between $250,000 and $1 million per year, and is given a well-defined topical research mission. The SRC Research Program includes 12 efforts funded at the Program level.

An SRC PROJECT supports the research of one to six faculty and graduate students and is usually funded at a level between $50,000 and $200,000 annually. Projects typically have a narrow focus with a three-year life expectancy.

Accountability

SRC research topics are assigned to universities through a system of formal contracts calling for deliverables on an agreed-to schedule. The universities receive funding on a cost-reimbursement basis that is keyed to recipients' meeting contractual obligations. Topics under study in university laboratories are sufficiently flexible to allow for innovation. While supporting the long-range needs of the industry, the SRC has developed a broad research strategy that is compatible with university culture. SRC technical staff, including several Industrial Residents, closely monitor each research task and work with industry representatives to offer hands-on guidance without permitting hands-on interference.

Each research activity sponsored by the SRC is reviewed annually by SRC staff and members of appropriate Technical Advisory Board (TAB) committees Reviews may include a single substantial research effort or an assessment of multiple smaller contracts and are usually conducted on campus. A typical review includes presentations of research results by faculty and student researchers. The progress is then critiqued by the TAB. The review process is extremely valuable to both the industry and to the university because technical interactions occur which generate discussion that aids in the process of maintaining a research program relevant to industry needs. Following the annual review, each contract's Principal (faculty) Investigator must submit a proposal for contract renewal. The science area TAB committees conducted 40 reviews in 1989, covering eighty-two contracts at forty-seven universities.

Participating Institutions

Arizona, University of
Arizona State University
Auburn University
Boston University
California at Berkeley, University of
California at Irvine, University of
California at Los Angeles, University of
California at Santa Barbara, University of
California at Santa Cruz, University of
California Institute of Technology
Carnegie-Mellon University
Case Western Reserve University
Clemson University
Colorado State University
Columbia University
Cornell University
David Sarnoff Research Center
Duke University
Florida, University of
Florida Institute of Technology
Florida State University
Georgia Institute of Technology
Illinois at Urbana/Champaign, University of
Lehigh University
Louisiana State University
Maryland, University of
Massachusetts at Amherst, University of
Massachusetts Institute of Technology
Massachusetts Microelectronics Center
Michigan, University of
Microelectronics Center of North Carolina
Minnesota, University of
New Jersey Institute of Technology
New Mexico, University of
North Carolina at Chapel Hill, University of
North Carolina at Charlotte, University of
North Carolina State University
Northeastern University
Ohio State University
Oregon Graduate Center
Princeton University
Purdue University
Rensselaer Polytechnic Institute
Research Triangle Institute
Rochester, University of
Rochester Institute of Technology
Rutgers, The State University
Sandia National Laboratories
South Florida, University of
Southern California, University of
Stanford University
State University of New York at Albany
Stevens Institute of Technology
Texas at Austin, University of
The Texas A&M University
Vanderbilt University
Vermont, University of
Virginia, University of
Wisconsin, University of
Yale University

Professor Ken 0. Wise
Director, SRC Center
for Automated Semiconductor Manufacfuring
at the University of Michigan

"... The SRC program was absolutely pivotal in the development of solid-state electronics at Michigan. The SRC commitment was key in convincing the University and the State to contribute significantly toward equipping our new fabrication facility. These contributions, in turn, allowed us to attract major additional funding. The result is a fully equipped, fully operational state-of-the-art facility with a doctoral student population that has increased by a factor of six in six years.

"... Research in manufacturing science ... has been an active, exciting area. No other research would have likely catalyzed so many joint projects among faculty from so many diverse areas; these interactions are multiplying and are an essential part of our program. There is no question that the SRC has been a real winner for Michigan."

The highlights of SRC projects given on the following pages are representative of the diversity, quality, and relevance of the research being performed.

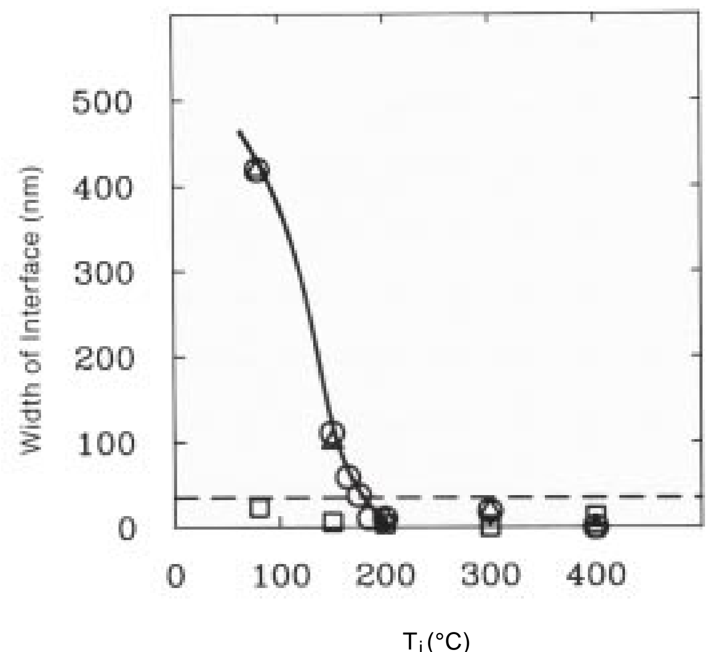
Polymer-Polymer Adhesion for First-Level Packaging

Polyimides are potentially excellent dielectrics for advanced first-level packaging applications, They have low dielectric constants and good planarizing characteristics They are also capable of being processed at much lower temperatures than alumina ceramics, thereby allowing the use of metals, such as copper, which have high conductivity but relatively low melting points. However, polyimides have important problems with polymer-polymer adhesion, making this an important issue in the reliability of multilayer dielectric systems.

Professor E.J. Kramer at Cornell, working in collaboration with scientists at the IBM Almaden Research Laboratories, has demonstrated that adhesion between layers of polyimide correlates with the intermixing of polymer chains at the interface between the two layers. When the zone of intermixing is relatively wide (e.g., > 100 nm) the adhesion is strong and vice versa. The reason is that the chains must entangle across the interfacing for a strong bond to result.

Professor Kramer has discovered that the processing parameters which most affect the intermixing are the extent of imidization (**f**) of the polyimide substrate and the presence of the solvent in the spinning process. A high f produced by a high imidization temperature, T,, causes the substrate to become highly immiscible with the spun-on layer of polyamic acid precursor. The solvent acts to dilute contacts between the partially imidized polyimide and the polyamic acid chains, thus widening the interface. The accompanying figure demonstrates these results

Professor Che-Yu Li
Cornell University



T_i (°C)

Width of interface formed between two layers of polyimide, showing that the width of the interface is strongly dependent on the presence of solvent and independent of a final heating to 400°C as long as the solvent is present.

Squares *represent interfaces produced without solvent after a final heating to 400°* C for one hour.
Circles *are spun-on layers with a final heating to 400°* C.
Triangles *are spun-on layers without a final heating to 400°* C.

Reference: S.F. Tead, E.J. Kramer, T.P. Russell, and W. Volksen, “Solvent and Curing Effects on Diffusion at Polyimide Interfaces” in *Electronic Packaging Materials Science,* Eds. K.A. Jackson, R. Jaccodine, and R.C. Sundahl, Mat. Res. Soc. Symp. Proc., Vol. 154, pp 239-248.

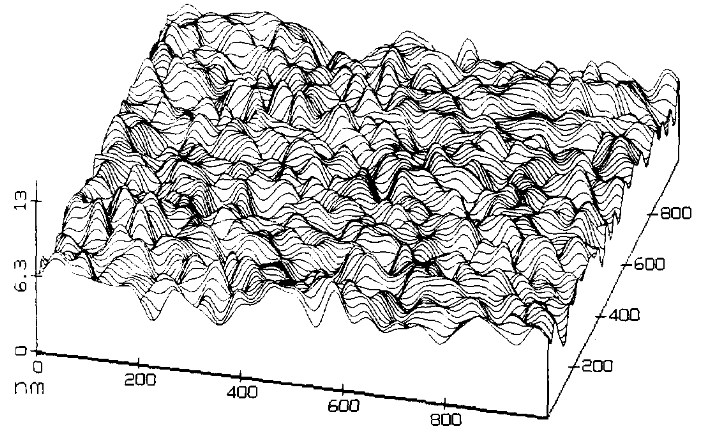
Low Resistance Silicon-Germanium Contacts

The use of germanium in silicon integrated circuit fabrication is being explored because of the potential for reducing the thermal budget for deep submicron device applications while providing certain beneficial properties. Rapid thermal chemical vapor deposition is being used to study the in-situ deposition of Ge, Si, SiO_2, and Si_3N_4. Epitaxial Ge and Ge-Si alloys can be deposited selectively at temperatures as low as 350°C.

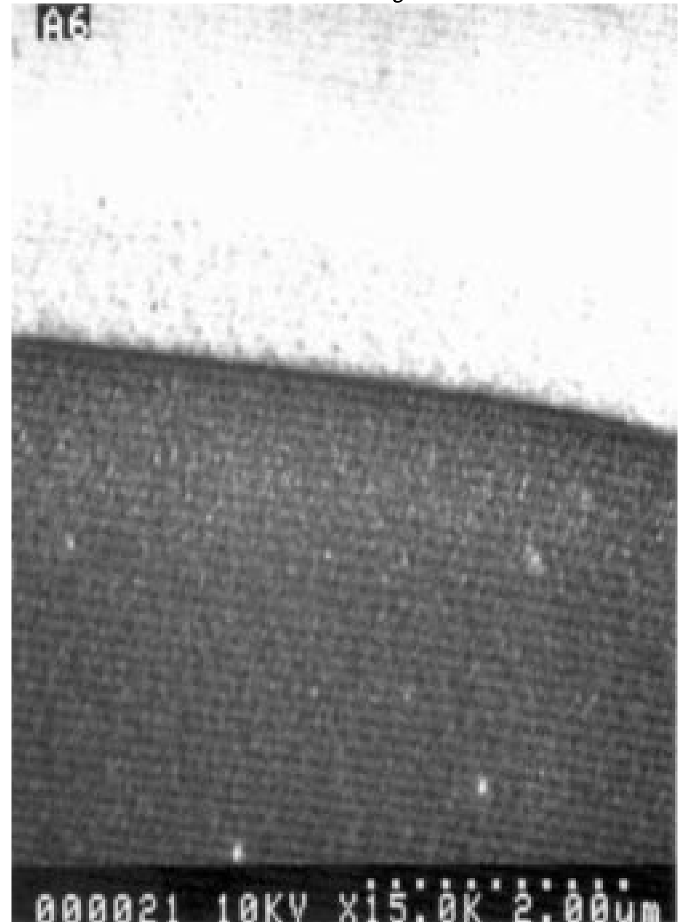
Germanium can be used as an intermediate layer between aluminum metallization and silicon contacts to reduce the contact resistance. It has been discovered that the deposition process is self-cleaning. In the rapid thermal process being employed, residual deposits of silicon dioxide on the contact surface are etched and removed as a gas prior to the selective epitaxial deposition of the doped germanium. The resulting specific contact resistance is 2 $\mu\Omega/cm^2$. Low resistance contact to the doped germanium is also expected to be possible through the formation of germanides of tungsten and titanium.

Germanium can also be deposited on silicon dioxide by first depositing a few monolayers of polysilicon. Polygermanium doped by ion implantation with boron can be activated at temperatures as low as 400°C.

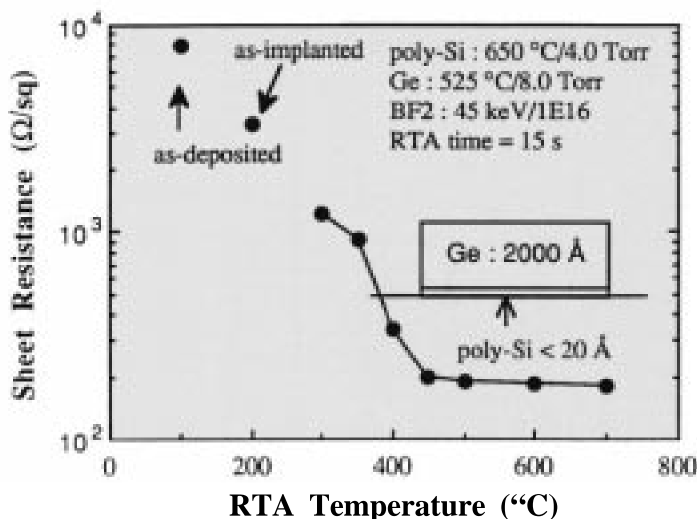
Professor J.J. Wortman
North Carolina State University



Surface of germanium epitaxially deposited on a silicon substrate at a low growth temperature of 350°C as revealed by a scanning tunneling microscope. The larger peak-to-valley distances are on the order of 30 angstroms.



SEM of doped germanium selectively grown at 425°C on a heavily doped silicon contact by rapid thermal processing. Lower growth temperatures result in a more uniform deposition.

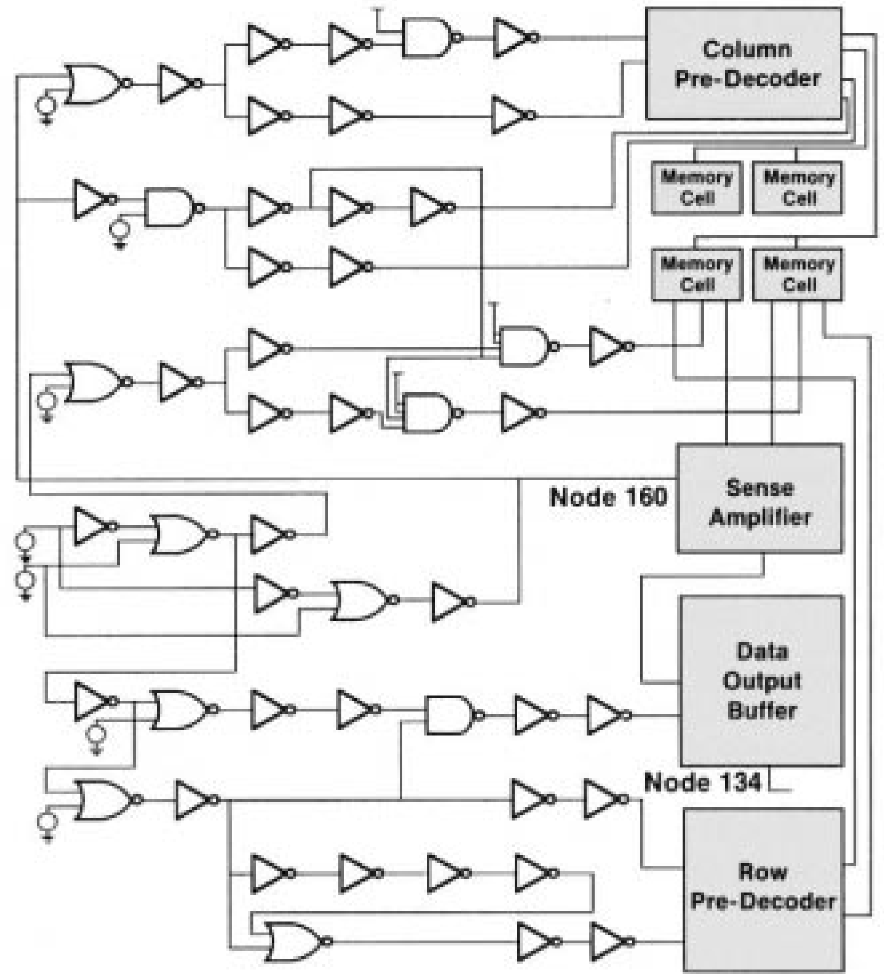


Sheet resistance of BF_2 implanted germanium deposited on SiO_2 by rapid thermal processing as a function of the process temperature.

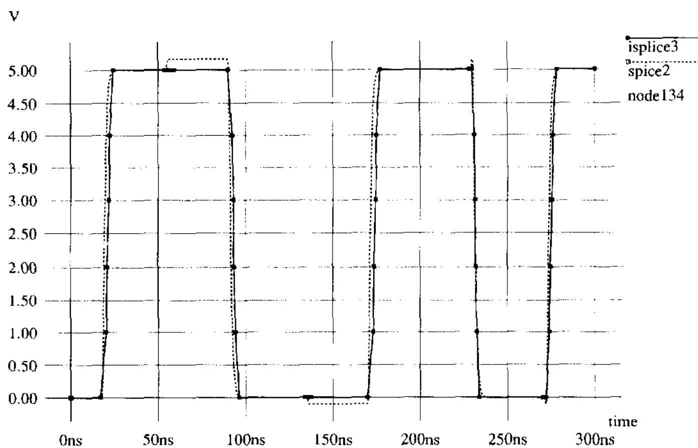
iSPLICE Mixed-Mode Simulator

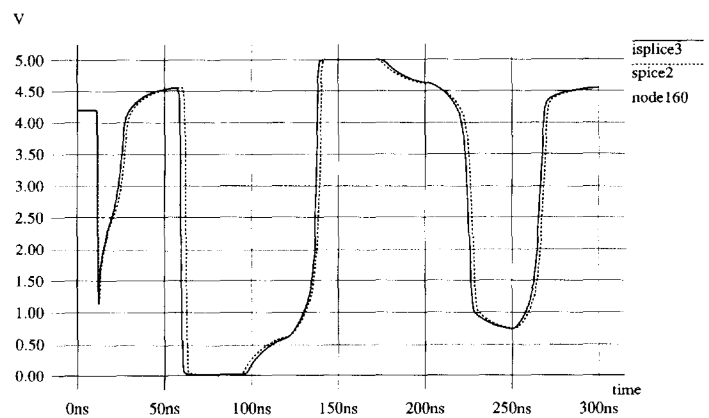
iSPLICE is a mixed-mode simulator that has been developed as part of the SRC research thrust in Reliable VLSI Architectures. The iSPLICE program combines event-driven electrical, logic, and electrical/logic techniques for accurate analysis of mixed analog/digital circuits. The program is roughly 40 times faster than SPICE with minimal loss of accuracy. The iSPLICE program is written in C and is available to SRC members from the University of Illinois.

Professor Resve A. Saleh
University of Illinois at Urbana-Champaign



CMOS static memory circuit containing approximately 300 transistors that was simulated using iSPLICE on a VAX 3500 workstation in 82 CPU-seconds compared to 3272 CPU-seconds required by SPICE2.





The two graphs show that resulting waveforms for two critical nodes of the simulated CMOS static memory circuit at top right are indistinguishable.

A Scattering Matrix Approach to Device Simulation

To address a pressing need for improved device simulation tools to treat carrier transport effects — important in modern devices, a scattering matrix approach is being developed as a new way to simulate devices. This approach promises the accuracy of Monte Carlo simulation with reduced computational burden. The new technique is especially well-suited to bipolar simulation, which poses special difficulties for Monte Carlo analysis. Quantum mechanical effects, increasingly important in ultra-small devices, can also be treated.

The scattering matrix approach has a strong physical basis. It begins by characterizing transport across a thin, Isolated semiconductor slab in terms of transmission and reflection coefficients which relate the emerging and incident fluxes by

$$\begin{pmatrix} b^+ \\ a^- \end{pmatrix} = \begin{bmatrix} t & r' \\ r & t' \end{bmatrix} \begin{pmatrix} a^+ \\ b^- \end{pmatrix} = \begin{bmatrix} S \end{bmatrix} \begin{pmatrix} a^+ \\ b^- \end{pmatrix},$$

where [S] is the scattering matrix (see Figure 1). For a slab with a given electric field and doping density, the scattering matrix is a rigorous description of carrier transport.

A typical scattering matrix for a thin silicon slab is illustrated in Figure 2. A semiconductor device is decomposed into thin slabs and analyzed by cascading the scattering matrices for each of the slabs. The contacts inject a known flux into the device and all other fluxes are obtained by the same techniques used for analyzing microwave circuits in terms of scattering matrices.

Figure 3 shows an example simulation for electron transport in a model device structure. The new approach correctly resolves the velocity over- and undershoot effects that occur at the electric field transitions. The average carrier density, velocity, energy, and even the distribution function, itself, can all be obtained from a scattering matrix simulation. The scattering matrix technique combines a first-principles approach to carrier transport physics with the computational efficiency required for engineering applications.

Professors Mark Lundstrom and Supriyo Datta
Purdue University

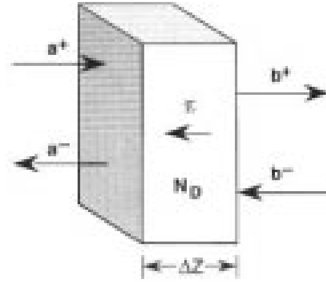


FIGURE 1. Definition of a scattering matrix to characterize electron transport across an isolated, thin slab of semiconductor. a^+ and b^- are the incident carrier fluxes and b^+ and a^- are the emerging fluxes.

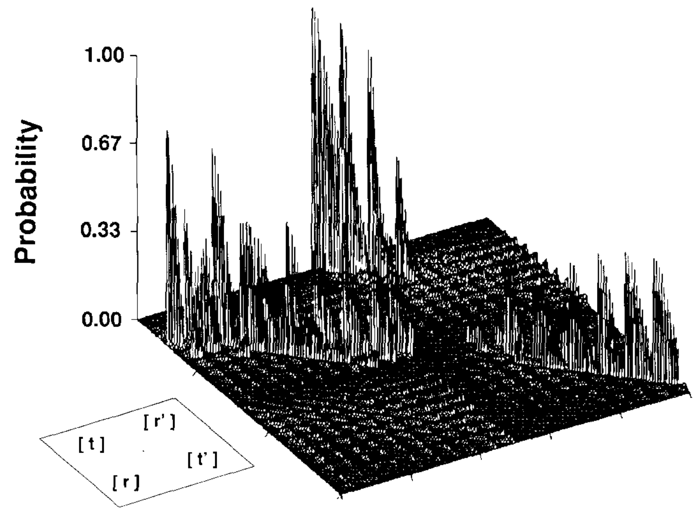


FIGURE 2. The scattering matrix for a silicon slab with 100 fluxes incident and emerging from each side of the slab. An electric field of 10^5 V/cm directed from right to left is assumed.

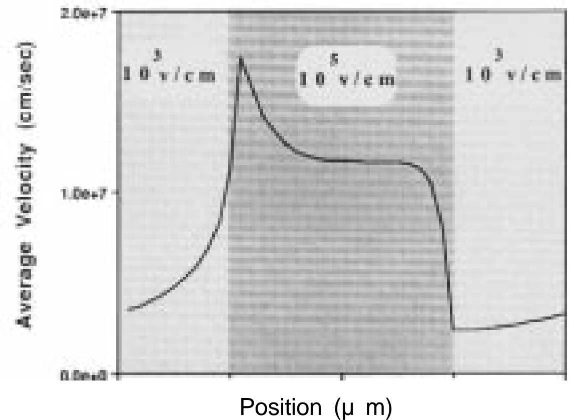


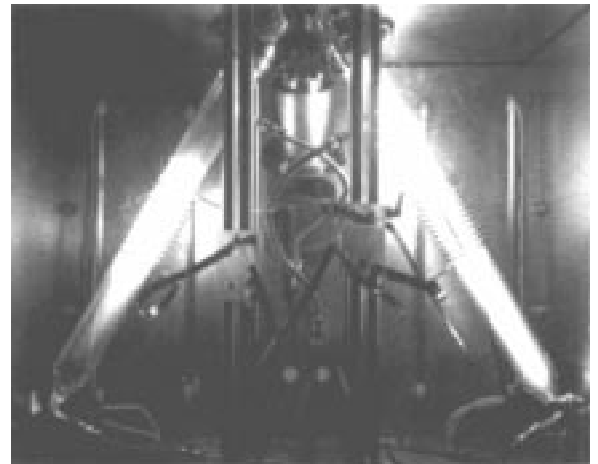
FIGURE 3. Average velocity versus electric field for electrons in a model silicon device structure as computed by the scattering matrix approach.

Remote Plasma-Enhanced Chemical Vapor Deposition (RPECVD) Reactor at Research Triangle Institute.

Advanced RPECVD Technology

The remote plasma-enhanced chemical vapor deposition (RPECVD) reactor shown in the photograph at the left is used for deposition of $SiO_2/Si_3N_4/SiO_2$ (ONO) gate dielectric stacks. This technology, under development at the Research Triangle Institute and North Carolina State University, allows integration of *in situ* cleaning, oxide deposition, and nitride deposition in a single process chamber; thus no wafer handling or environmental exposure occurs between cleaning and critical interface formation. Cleaning and deposition are carried out at 300°C. The resultant structures exhibit Si/SiO_2 interface state density and fixed charge values equal to thermal oxides, and charge-to-breakdown results in excess of 150 coulombs/cm^2 at a composite thickness of 65 angstroms.

Mr. Robert J. Markunas
Research Triangle Institute



The plasma enclosure of a dual source, remote plasma-enhanced chemical vapor deposition (RPECVD) reactor at the Research Triangle Institute. Selective activation using individually tailored conditions in the separate plasma sources provides enhanced process control in the formation of multicomponent material structures.

Comprehensive Ion Implant Models

As feature sizes in integrated circuits approach the deep submicron range (< 0.35 μm), extremely compact doping profiles are increasingly required. In ion implantation, greater difficulties exist due to increased channeling of ions in the lattice that occurs at lower implant energies, in particular for boron. Moreover, complete experimental data and accurate models do not exist for implanted impurity profiles as a function of both implant angles and dose in addition to energy. These accurate models are needed in order to understand how to optimize device structures and process control in manufacturing.

A two-prong research approach is being used to develop the needed models for the ion implanted impurities commonly used (B, BF_2, As, P), Extensive experimental work to “map” the implant profile dependence on tilt and rotation angles has been performed, an example of which is shown in Figure 1. For the first time, the dependence of boron ion channeling over all angle space in a 0° to 10° tilt angle range and for all rotation angles (0° to 360°) has been obtained. An example of this mapping is illustrated in Figure 2. The other major part of this effort is the development of an accurate theoretical Monte-Carlo-based model for simulating as-implanted profiles, When completed, this model will be primarily used to provide the parameters for a computationally efficient model based on the use of two Pearson distribution functions.

Professors A.F. Tasch and D-L. Kwong
University of Texas at Austin

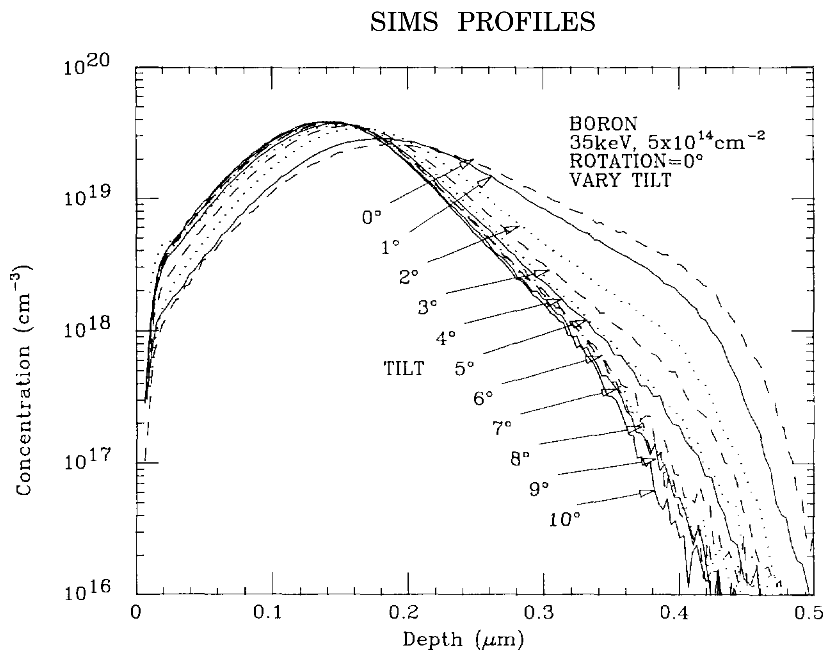


FIGURE 7. Implanted boron profiles in silicon as a function of tilt angle at 0° rotation angle.

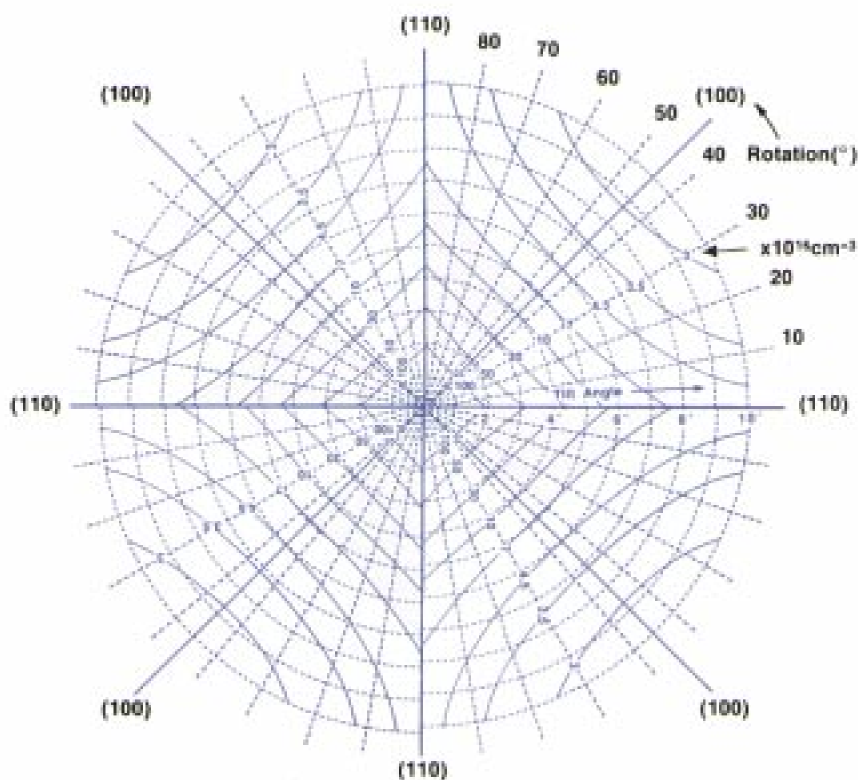


FIGURE 2. Boron concentration at 0.4 μm depth in silicon as a function of tilt and rotation angle (35 keV, $5x10^{14}cm^{-2}$ dose). The contours are isoconcentration contours which illustrate the strong dependence of channeling on tilt angle and lesser dependence on rotation angle.

BSIM2 (Berkeley Short-channel IGFET Model version 2.0)

BSIM2 is designed to meet the challenge of digital and analog circuit simulations in the 1990s. It has been thoroughly calibrated for MOS transistors with channel lengths as small as 0.2 μm and gate oxide thicknesses as thin as 8.6 nm. In BSIM2, all currents and charges and their first and second derivatives are continuous with respect to the terminal voltages. As a result, BSIM2 can be more robust than much simpler models in transient analysis. Extraction of the model parameters is made easy by a custom-automated parameter extractor written in C language for an IBM PC (or compatible)/HP4145 platform. A simple, multistep algorithm is used to reduce parameter optimization time and improve modeling accuracy.

Professor Ping K. Ko
University of California at Berkeley

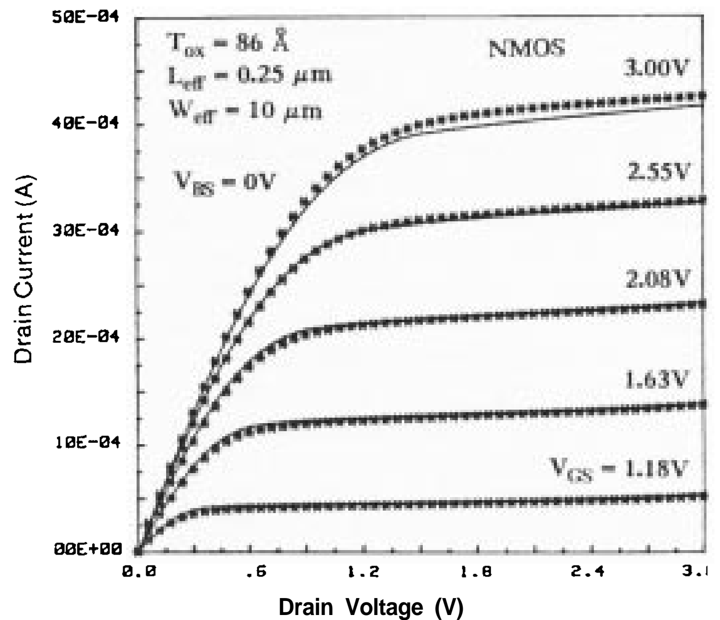


FIGURE 1. The IDS- VDS characteristics as modeled by BSIM2 for a 0.25 micrometer NMOS transistor. Modeling results are shown as solid lines, and the asterisks are measured points.

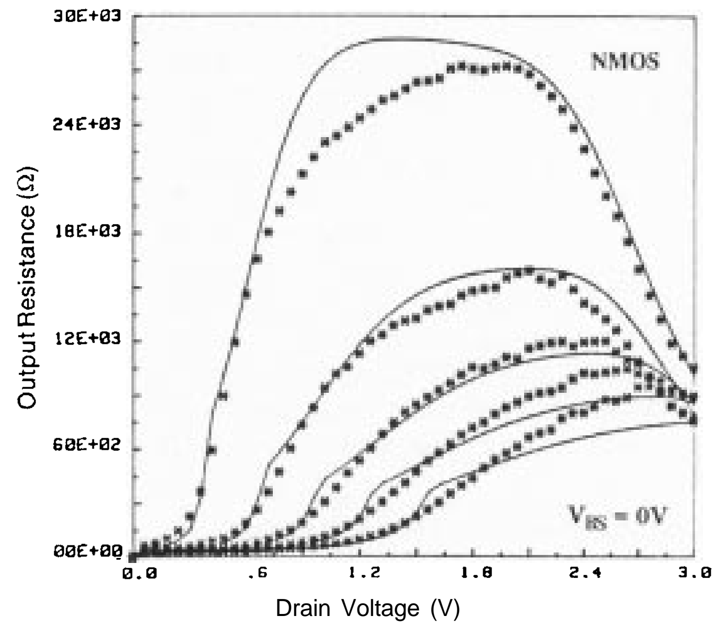


FIGURE 2. The output resistances of the device shown in Figure 1. Modeling results are shown as solid lines, and the asterisks are measured points. Accurate modeling of the output resistance is necessary for analog circuit simulations.

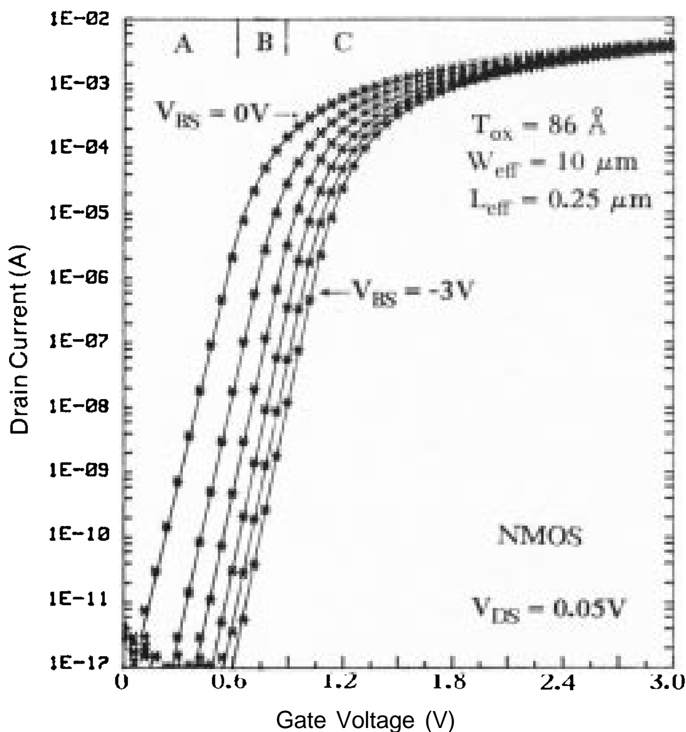


FIGURE 3. The subthreshold characteristics for the device shown in Figures 1 and 2. BSIM2 takes into account the inversion-layer thickness and uses a Spline function to generate a smooth transition (region 6) from weak inversion (region A) to strong inversion (region C).

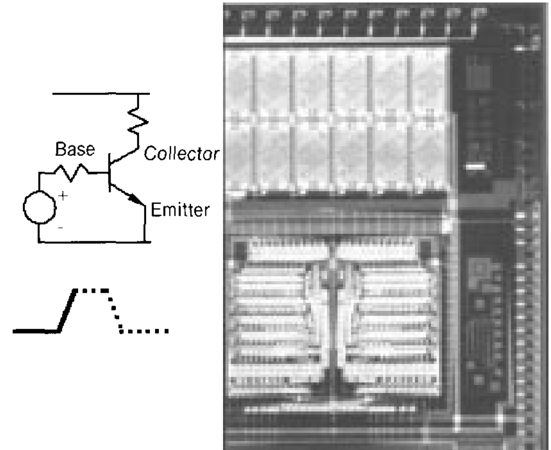
Visualization

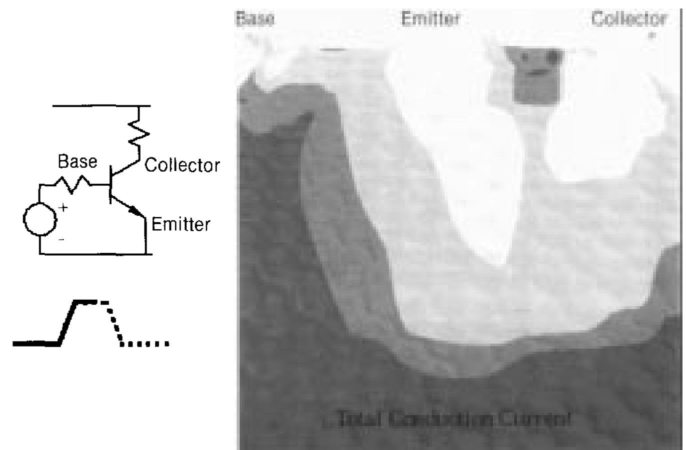
Visualization technology has been incorporated into the Stanford process and device modeling tools, SUPREM and PISCES, resulting in remarkable new capability for these programs. Using the public domain visualization software package ImageTool from the National Center for Supercomputer Applications at the University of Illinois, animated color video displays of simulations of process flows and device transient response can be produced on common engineering workstations. The penalty for this visualization processing typically runs on the order of less than 10% of the total CPU time.

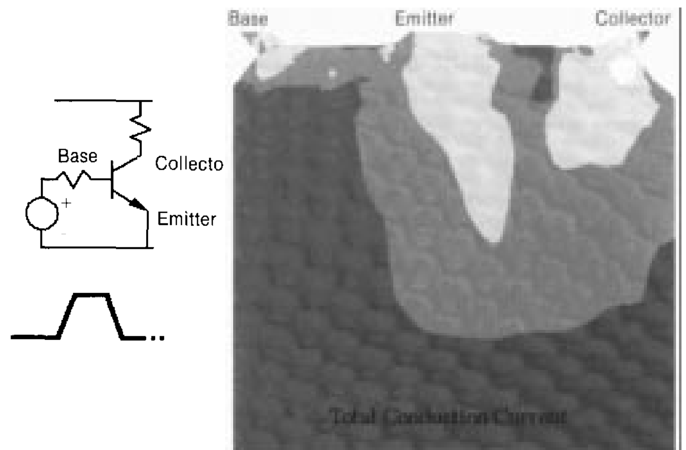
The accompanying pictures illustrate some simple examples of this capability, although the absence of color and animation in these still frames masks much of the detail and lacks the capability of a video monitor. These frames are from a transient simulation of the NPN device turning on and off. The colors (shown here as a gray scale) correspond to the current density, with the lighter colors corresponding to higher current densities. Experience with this output technique shows that the enormous volumes of information generated by these simulation tools can be displayed in a form that is highly visible and easy to comprehend.

Animation, in particular, has been found to help identify small but significant variations which would otherwise be extremely difficult to detect. Even highly experienced users have seen new features in simulation results which are presented in animated color visualization form. Releases of both SUPREM and PISCES that include these visualization features are expected to be made available in the near future.

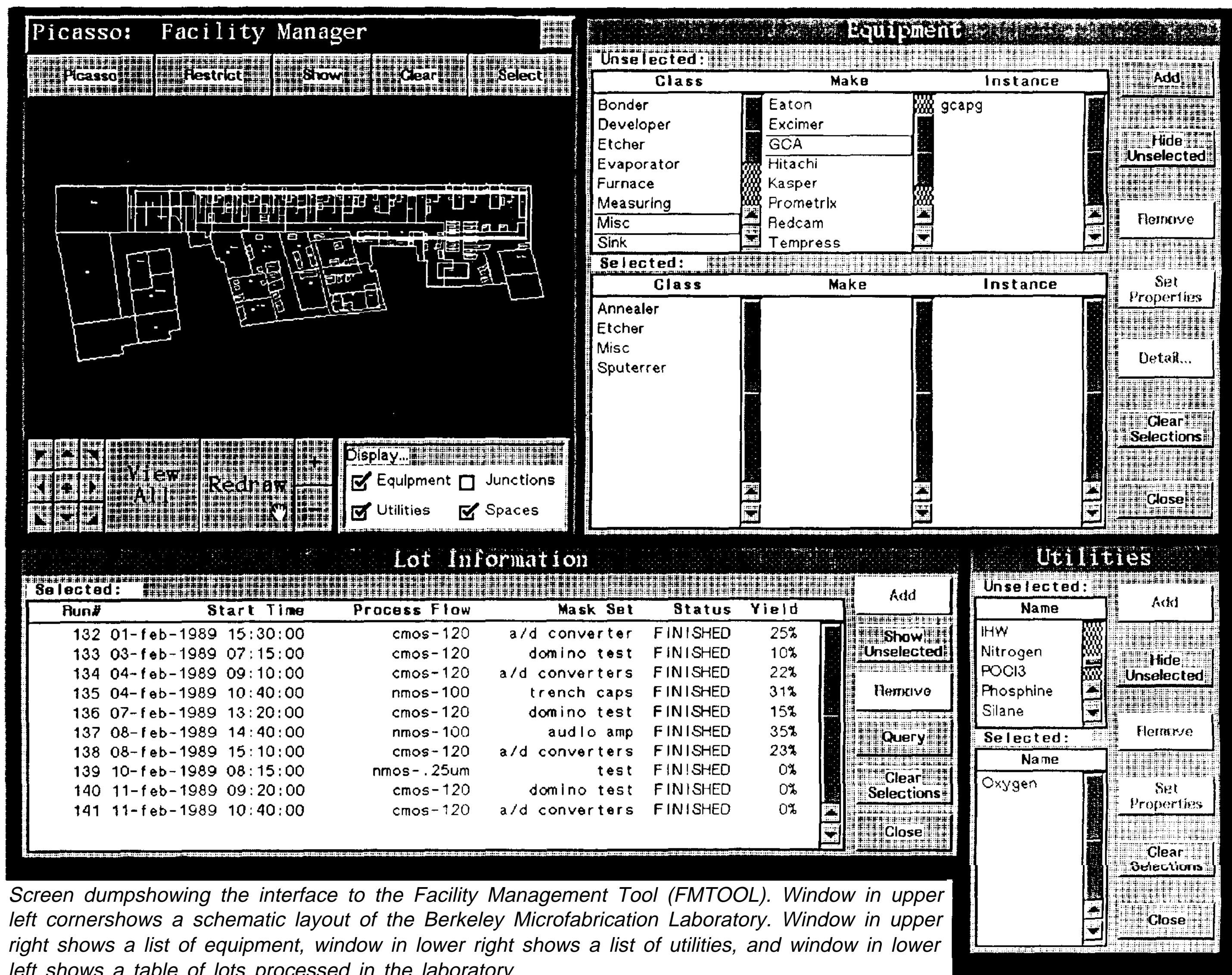
Professors Robert W. Dutton and James D. Plummer
Stanford University







Series of three still frames from a transient simulation of the NPN device turning on and off that would be viewed in color and with animation when using the visualization technology described above.



Screen dumpshowing the interface to the Facility Management Tool (FMTOOL). Window in upper left cornershows a schematic layout of the Berkeley Microfabrication Laboratory. Window in upper right shows a list of equipment, window in lower right shows a list of utilities, and window in lower left shows a table of lots processed in the laboratory.

The Facility Management Tool

One of several goals for the Integrated CAD/CAM/CAT for VLSI project at the University of California at Berkeley is to develop and demonstrate improved software for company-wide production planning and for factory floor scheduling of the fabrication, assembly, and test of semiconductor products. The Facility Management Tool (FMTOOL), developed as part of this project, allows operators, equipment and process engineers, and managers to browse data about equipment, utilities (e.g., water lines), spaces (e.g., rooms) and lots. FMTOOL provides a graphical user interface through which queries can be entered that involve conventional business data (e.g., lot history), engineering data (e.g., physical measurements or test results), geometric data (e.g., equipment connected to a utility), and spatial data (e.g., equipment within a room). When using the FMTOOL software, complex queries are specified by selecting items with a mouse and/or filling in a form. Example queries include “fetch all lots processed by a particular piece of equipment” and “highlight the equipment connected to the oxygen line that processed a particular lot.”

Professor Lawrence A. Rowe
University of California at Berkeley

Extending the Limits of Optical Lithography

Despite continued predictions to the contrary, optical lithography continues to be the lithographic technology of choice for ULSI manufacture. Thus, one of the key questions facing the industry is the extent to which optical lithography should be employed before switching to a suboptical technology, such as X-ray lithography.

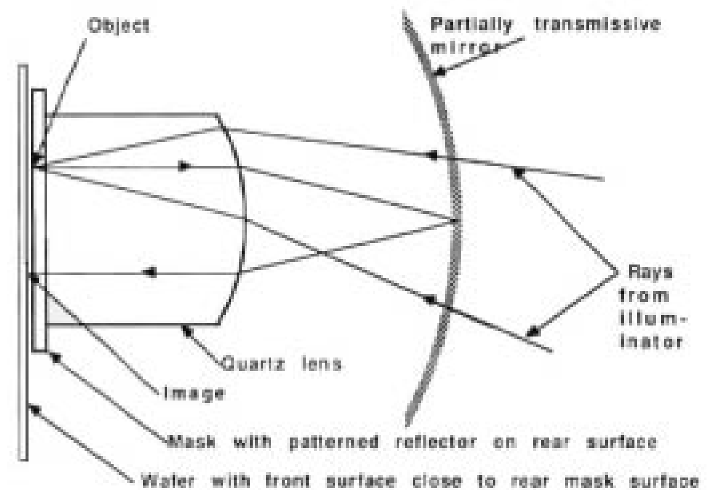
A highly original configuration, which might well make possible the extension of optical lithography to handle 256 Mbit DRAM technology, was recently proposed by David A. Markle. This configuration, shown in the photo and described beneath the accompanying diagram, should allow high numerical aperture (0.7) for diffraction-limited operation over an enormous field of view (14 x 28 mm^2).

Key questions include the basic operation of the optics, obtaining adequate contrast from the reflective mask, maintaining focus at this very high numerical aperture, and the ability to make adequately precise 1 X masks for 0.25 μm design rules.

A prototype to prove out the concept has been designed and constructed and is being brought on line at Stanford. This prototype employs only spherical surfaces and has a relatively restricted field of view (4 mm diameter) but will allow evaluation of the concept.

Professor R. Fabian W. Pease
Stanford University

Prototype 'Half-Field Dyson' optical system, emphasizing the compactness and simplicity of this approach (photograph courtesy of A. Walther).



Schematic view of essential parts of the 'Half-Field Dyson' projection system presently being brought on line at Stanford. In the final version, the single quartz lens is to be replaced with a triplet; and the gap between wafer and mask and between mask and lens will be more than 0.7 mm. The unusual features of this configuration are:

1. *mask operates in reflection so wafer is stepped just behind the mask;*
2. *illumination is brought in through the partially transmissive main focusing mirror;*
3. *as a result of 1 and 2, design can take full advantage of the original Dyson concept without vignetting at high numerical aperture (unlike the Wynne-Dyson arrangement presently used in commercial steppers);*
4. *illumination is the 248 nm line of a conventional mercury arc instead of the much more costly line-narrowed excimer lasers typically employed in deep ultra-violet steppers.*
5. *reflective mask is configured so that its quartz substrate also acts as a pellicle, thus protecting the mask pattern from the ambient;*
6. *needs only four projection optical elements instead of more than fifteen required by refractive systems;*
7. *alignment of the optics is enormously simplified both because of their small number and the concentricity of the focusing surfaces.*

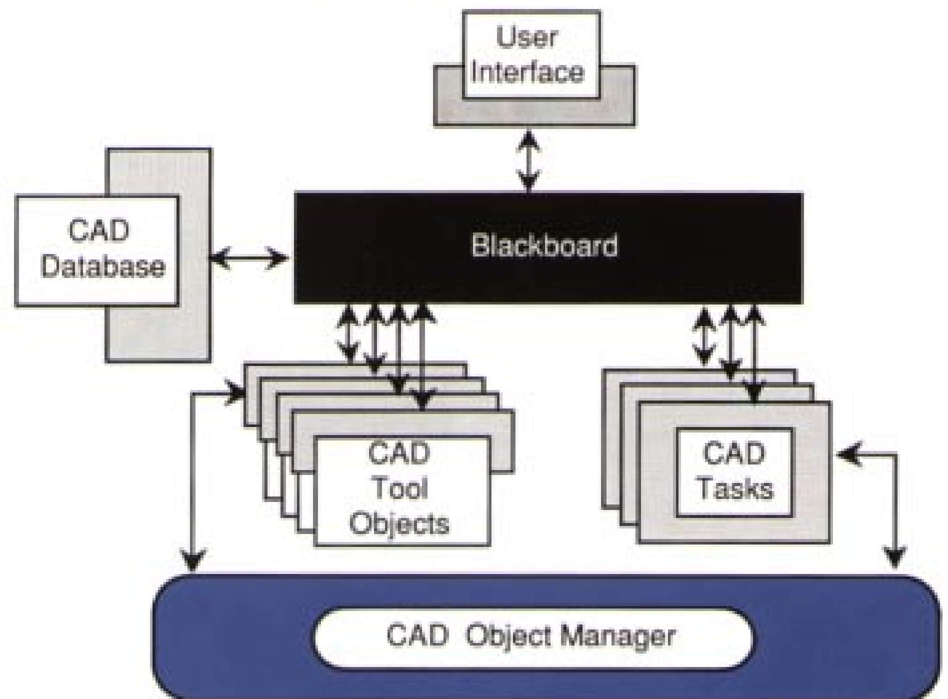
The TimberWolf Automatic Layout Package

The TimberWolf software package consists of automatic layout programs for the macro cell, standard cell, mixed macro/standard cell, gate array, and sea-of-gates design styles. TimberWolfMC, the macro cell layout program, produced the smallest chip area on a set of standard benchmark circuits.

New features added in 1989 include a macro-cell, graph-based global router that outperforms existing algorithms and an approach to full-chip detailed routing that avoids the need for a channel definition step. Timing-driven placement is featured for both the macro cell and the standard cell placement programs. The user may specify lower and upper bounds for the lengths of any number of signal paths in the network. A new approach to timing-driven, mixed macro/standard cell layout of very large circuits was also developed in 1989; and a new sea-of-gates-specific global router produced results significantly better than those previously reported for both gate array and standard cell benchmark circuits.

Professor Carl Sechen
Yale University

The CADWELD Framework



The CADWELD Design Framework

Increasing complexity of the VLSI design process has motivated the need for a computer-aided design (CAD) framework that can integrate a set of heterogeneous CAD tools. Research in this project has focused on the design methodology management aspects of frameworks and has resulted in the CADWELD VLSI Design Framework. CADWELD employs an object-oriented tool integration scheme that can support dozens, or even hundreds, of tools. In this scheme, CAD tools are encapsulated as strongly typed objects within a hierarchical classification leading to a powerful and expressive modeling mechanism. These objects interact with the designer and CAD Tasks (an encapsulated set of design steps) through a "blackboard." This approach allows a large population of tools to share a common graphical control and communication mechanism as well as making CAD tools easier to learn and maintain.

Professor Stephen W. Director
Carnegie-Mellon University

Selective Epitaxial Silicon Growth

A new technique called Confined Lateral Selective Epitaxial Growth (CLSEG) is used to form thin films of single crystal silicon-on-insulator (SOI). The CLSEG process can be used either for local SOI films suitable for individual devices with an optional substrate connection or for whole-wafer SOI films where complete dielectric isolation is desired.

The fabrication of CLSEG begins by forming the structure shown in Figure 1 (a). First, a bottom layer thermal oxide is formed on a <100> silicon substrate, and patterned to form a seed hole oriented along (001) equivalent directions. A sacrificial layer of CVD amorphous silicon has been deposited, masked and etched. The height and lateral dimensions of the etched sacrificial layer establish the height and shape of the CLSEG silicon. The top layer is deposited and etched to form via holes which expose the sacrificial layer. The top layer material is CVD silicon nitride and is deposited after the amorphous silicon has been made poly and oxidized to form a thin thermal oxide layer.

Figure 1(a) shows the sacrificial layer completely removed by using a wet silicon etch, leaving behind an empty cavity with dielectric walls. The cavity is filled with selectively grown single-crystal silicon, grown from the seed hole, as shown in Figure I(b). As the growing silicon encounters the cantilevered top layer, growth is confined and must proceed laterally, forming a local SOI slab of device-quality silicon. Layers of more than 10 μm have been grown over the bottom oxide with films of 0.25 μm to 1.2 μm thick.

Professor Gerald W. Neudeck
Purdue University

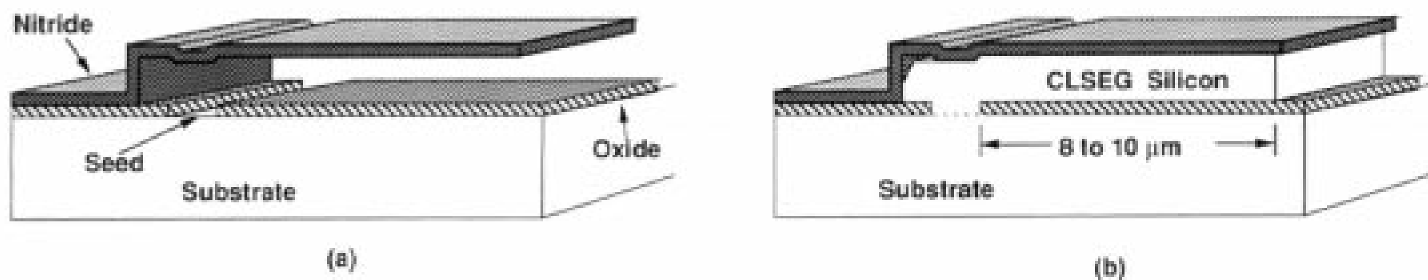


FIGURE 1. Fabrication steps in Confined Lateral Selective Epitaxial Growth (CLSEG). Structure (a) shows an empty cavity formed by use of a sacrificial layer of chemical-vapor-deposited amorphous silicon. Structure (b) shows the cavity filled with selectively grown single-crystal silicon.

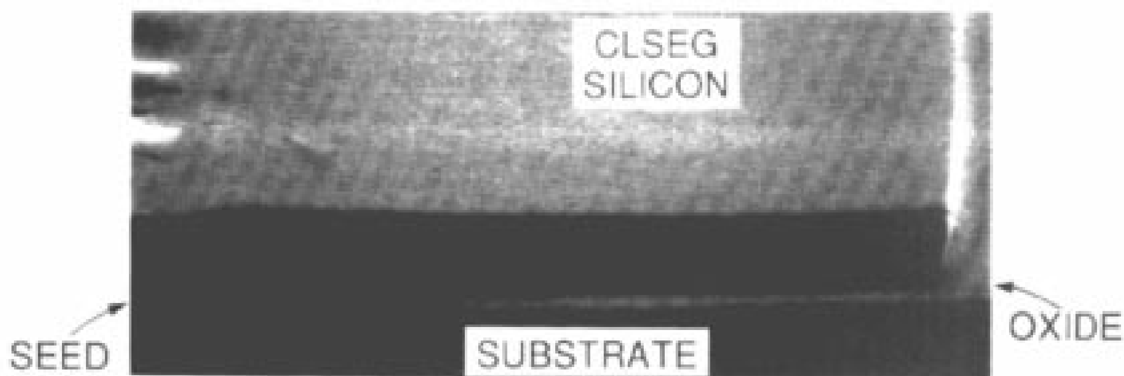


FIGURE 2. SEM of the grown CLSEG.

SRC
COOPERATIVE RESEARCH

Technology Transfer

Implementing Results of the SRC Research Program

The SRC has made a strong commitment to the transfer of technology from its Research Program to its sponsoring companies and government agencies. The usual mechanism of research disclosure by universities is peer-reviewed publications and/or presentations More than 850 preprints and reports from university researchers were added to the SRC library in 1989, and nearly 17,000 requests for copies of university documents were received from industry/ government participants. However, to facilitate the rapid utilization of research results by industry, the SRC's experience is that technology transfers best through interaction between the end-user who has a direct need for the results and the researcher who has obtained the results.

To facilitate direct contact between industry personnel and university researchers, the SRC throughout its seven-year history has used a “small meeting” approach to assemble groups of 20 to 125 representatives from industry, government, and academia. In 1989, eighty-seven “small meeting” events were sponsored by the SRC, including:

- Four WORKSHOPS at which technical experts from across the nation explored the state-of-the-art and future needs in Design for Manufacturing, Process Engineering, CAD Frameworks, and Computer-Integrated Manufacturing for Integrated Circuits to crisply define research issues and the elements of a new or expanding research task.
- Four TOPICAL RESEARCH CONFERENCES, with an average attendance of 100 persons, at which specialists from the SRC community discussed leading-edge research in Plasma Etching, High-Level Synthesis, Silicon-Based Epitaxial Technologies, and BiCMOS
- Two VIDEO CONFERENCES — on Design Synthesis and Integrated Technology Modeling for IC Process/Device Design — which were conducted at the request of the SRC Technical Advisory Board to exploit the video broadcast media for efficient and timely information distribution to large groups of industry scientists and technicians.

Technology transfer taking place at an SRC review at Purdue University between James W. Siekkinen, Ph.D. student and SRC Fellow, and George V. Rouse, Principal Engineer at Harris Corporation.

- Forty CONTRACT REVIEWS AND KICKOFFS at which representatives from industry and government joined members of the SRC corporate staff in reviewing or initiating one or several research projects on university campuses.
- Six TECHNOLOGY TRANSFER COURSES and several technical briefings conducted at university campuses to acquaint industry and government scientists/engineers with new software packages and other technical innovations.

- A VIDEO LECTURE SERIES was implemented in 1989 to tape presentations by selected university faculty, who described research results and potential applications. These and tapes from SRC video conferences are available to industry and government participants through the SRC's new Video Library.

A Mentor Program was conceived by the Technical Advisory Board and inaugurated by the SRC in 1983. Through this mechanism, a scientist or engineer from a member company or participating government agency can establish an active, constructive interface with a faculty investigator from an SRC research contract. In 1989, more than 400 Mentors participated in this program, offering guidance to the research effort and transferring innovative knowledge to member sites.

Since its inception, the SRC has provided the opportunity for member company and government agency personnel to join the technical staff at SRC headquarters for periods of one to two years. This residency program provides valuable experience in relevant technologies and technology transfer. Working with the SRC staff, the residents contribute industry perspective to the research effort and participate in monitoring the research contracts. Six industry employees were in residence on the SRC staff in 1989 and made a significant contribution to the success of the Research Program. Having an employee on site for continuous access to the research results is an excellent mechanism for maximizing the benefits of SRC membership.

Electronic connectivity for communication among members of the SRC community doubled in 1989, both through use of the SRC's Information Central database and the INTERNET network.

Relevant education for students who will graduate to employment by companies in the U.S. semiconductor industry or by U.S. universities remains one of the major objectives of the SRC. More than 600 graduate students, including 34 with SRC Fellowships, carried out research under SRC contracts in 1989. Of the students receiving degrees after working on SRC research, 70% gained employment in the SRC industry/government/academic community, many acting as agents for technology transfer by continuing their research.

Dr. Edward L. Hall
Manager, TCAD Department, Semiconductor Products Sector, Motorola, Incorporated

"Motorola was one of the companies that helped establish the SRC in 1982, and we have been very active since that time in making sure the SRC is beneficial to us. Periodically, we do a cost-benefit analysis on our membership in the SRC, and we have found that this cooperative venture has been one of the best external investments we have made. Every year, the return on that investment has increased. Each year, more and more Motorola engineers and researchers participate in the many SRC programs and bring back to Motorola SRC-funded results. We actively recruit SRC graduate students both for 'summer' positions and for full-time employment. This cooperative research effort has paid off for our company and, I believe, for our industry."

Future Directions

Needs, Opportunities, and Responses

Guided by its members as well as the university research community with which it works, the SRC continues to identify needs and opportunities in semiconductor research, and the resources for appropriate responses. Priorities are established through goals and budgets while retaining the flexibility to seize opportunities and to search unmapped technologies for the rare finding that causes a paradigm shift.

Looking toward the next decade, the largest contribution of SRC's research will be to the continuing climb up the trend lines toward better performance of industry semiconductor products. Described in terms of function, quality, speed, complexity, or any of the other parameters associated with integrated circuits, the advancement of the base technologies upon which these trends depend must have the highest priority in SRC research. They comprise the existing knowledge base upon which the industry relies. Included are multilayer interconnections, pattern transfer methods, design and manufacturing tools, fabrication technologies, and other ingredients of the product definition and production methods of today's industry.

Beyond the base semiconductor technologies are those technologies, methodologies, and design approaches that may cause significant deviations from the trends, i.e., paradigm shifts. Examples may be found in new system design approaches, a new type of device substrate (such as SOI), or radically different approaches to pattern transfer. More than likely, they cannot be identified until they are discovered. The relatively unconstricted nature of university research provides the most fertile ground for nurturing creativity, and it may be the most important of the SRC's products.

In the coming year, the SRC will seek to continue to improve its mapping of the technology future, the productivity of its research, its leadership in semiconductor research, and the search for the unpredicted results that may make the greatest difference.

TAB, UAC and GCC

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SEMICONDUCTOR RESEARCH CORPORATION
POST OFFICE BOX 12053
RESEARCH TRIANGLE PARK, NC 27709
(919) 541-9400

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