
**RESPONSE TO REQUEST FOR INFORMATION**

Department of Commerce

National Institute of Standards and Technology

Submitted via: *MfgRFI@nist.gov*

**In response to:**

Request for Information: Manufacturing USA Semiconductor Institutes

Agency/ Docket No. 221004-0210

**Submitted by:**

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**About SRC (Semiconductor Research Corporation, SRC.org):** Established 40 years ago, SRC is a non-profit public-private partnership for semiconductor research consisting of 27 industry members, 3 government agencies, and over 100 universities. Together, they have created the technologies and trained the workforce to support the semiconductor industry with over $2B of sponsored research.

# Summary

The CHIPS Act is making history. The passage of the CHIPS Act is both a great opportunity to accelerate the US semiconductor industry and also a great responsibility to ensure that the funding is used wisely to address the opportunities defined by both NIST and Congress. This is a once in a generation opportunity to redirect and propel the industry and we must get it right.

Semiconductor Research Corporation (SRC), on behalf of our industry members and academic partners, is pleased to submit this response to NIST's Microelectronics Manufacturing USA Institute (MMI) RFI. To effectively create and operate an MMI aligned with the goals of the RFI and to strengthen the Microelectronics and Advanced Packaging Technology (MAPT) innovation ecosystem including materials, design, fabrication, advanced test, assembly, and packaging capability, the Institute must manage R&D programs that effectively create technology that enables US manufacturing in the years to come. This requires successful technology generation and its transfer into industry as well as scaling education and workforce development (EWD) programs to provide skilled candidates to fill tens of thousands of US semiconductor engineering jobs in next 5-10 years.

*"Getting the R&D infrastructure right will determine our success for decades."*

-Commerce Secretary Gina Raimondo, Industrial Advisory Committee meeting Dec. 8, 2022, Washington D.C.

The US Semiconductor industry faces unique challenges: low (11%) global semiconductor fabrication capacity, weak (3%) global packaging capacity, and no advanced node (5 nm and below) on-shore fabrication facilities. In this RFI response, SRC and our partners have identified and described recommendations for creating and operating an MMI to help solve these problems and to "Connect people, ideas, and technology to:

- Solve industry-relevant advanced manufacturing challenges
- Enhance industrial competitiveness and economic growth
- Strengthen our national security[1]"

[1] Dr. Kelley Rogers, NIST, Manufacturing USA Semiconductor Institute Request for Information Webinar October 20, 2022

# Key Points Summary

1) CHIPS Act R&D programs must create new capabilities that are designed concurrently to ensure a sustainable ecosystem is established for the entire innovation pipeline. **(Figure 1)**
    a) Technology must have a pathway to span from Basic Research through Demo & Scale to reach technology transition and deployment without falling into Valleys of Death
    b) The impact of CHIPS R&D will be maximized when R&D programs across government are designed to integrate. The MAPT Institute should create technology that feeds explicitly and intentionally into NSTC, NAPMP, NIST Metrology, DOD Commons, and existing R&D programs
    c) Grow existing infrastructure by scaling effective models and filling existing gaps
2) The MAPT Institute must be a convening epicenter governed by a transparent and inclusive membership model with broad membership for collaborative, high impact R&D and workforce development, prioritizing public interests including:
    a) all aspects of the supply chain from materials suppliers through systems integrators
    b) industry, academia, government, trade organizations, and beyond
    c) domestic and international companies from start-ups through industry titans, both domestically and from like-minded nations supporting US manufacturing
    d) a distributed network of higher education that spans vocational/ trade schools and community colleges through tier 1 research universities, minority serving institutions, underserved communities, veteran training, reskill/upskilling.
3) Institute technical direction and scope should be industry led, and therefore Microelectronics and Advanced Packaging Technology (MAPT) must be kept together within one institute.
    a) Complementary R&D of MAPT topics will maximize system performance, cost, and commercial relevance
    b) Unification the community, industry, and academia for maximizing impact
    c) Provides value to the community such that it can be perpetually supported without extensive government resources
4) The MAPT scope requires the resources of a super-sized Institute.
    a) The breadth and scope of a MAPT institute requires at least $250M/year total, including cost-match
    b) MMI should allocate most financial resources to performing R&D, education and workforce development, and technology transfer with few financial resources used for overhead or management fees. Overhead rates should be capped at 10%.
    c) A super-size institute's risk should be mitigated by scaling existing R&D models that work effectively instead of creating a new model

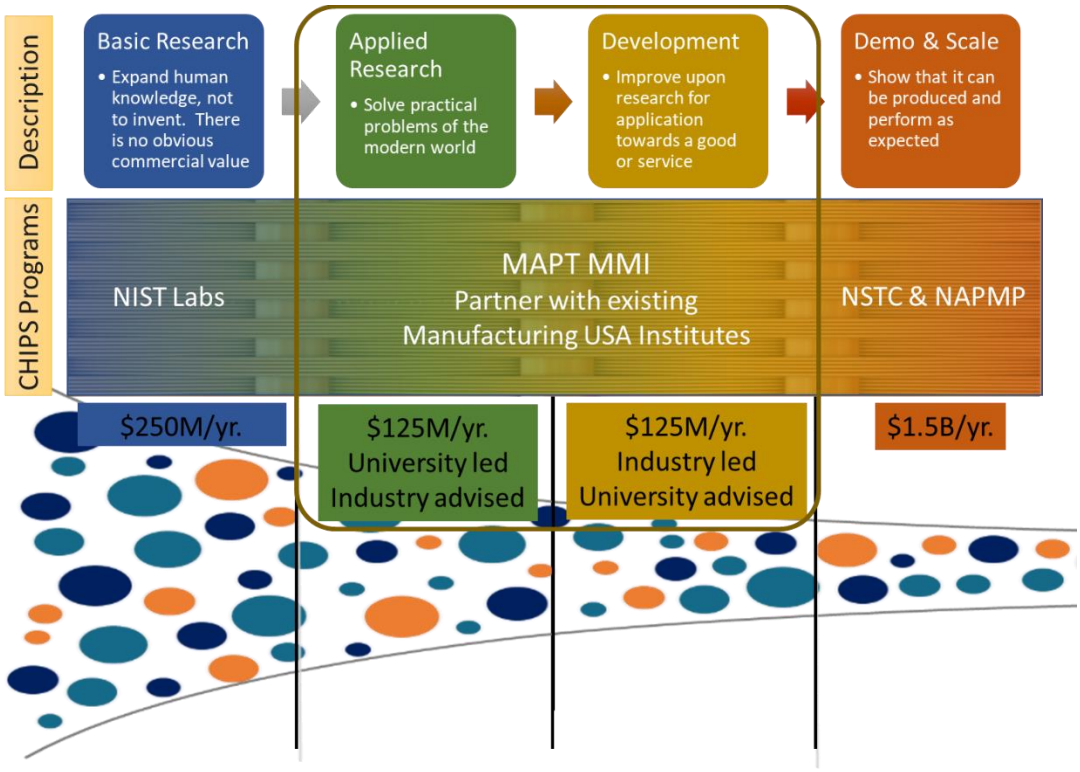


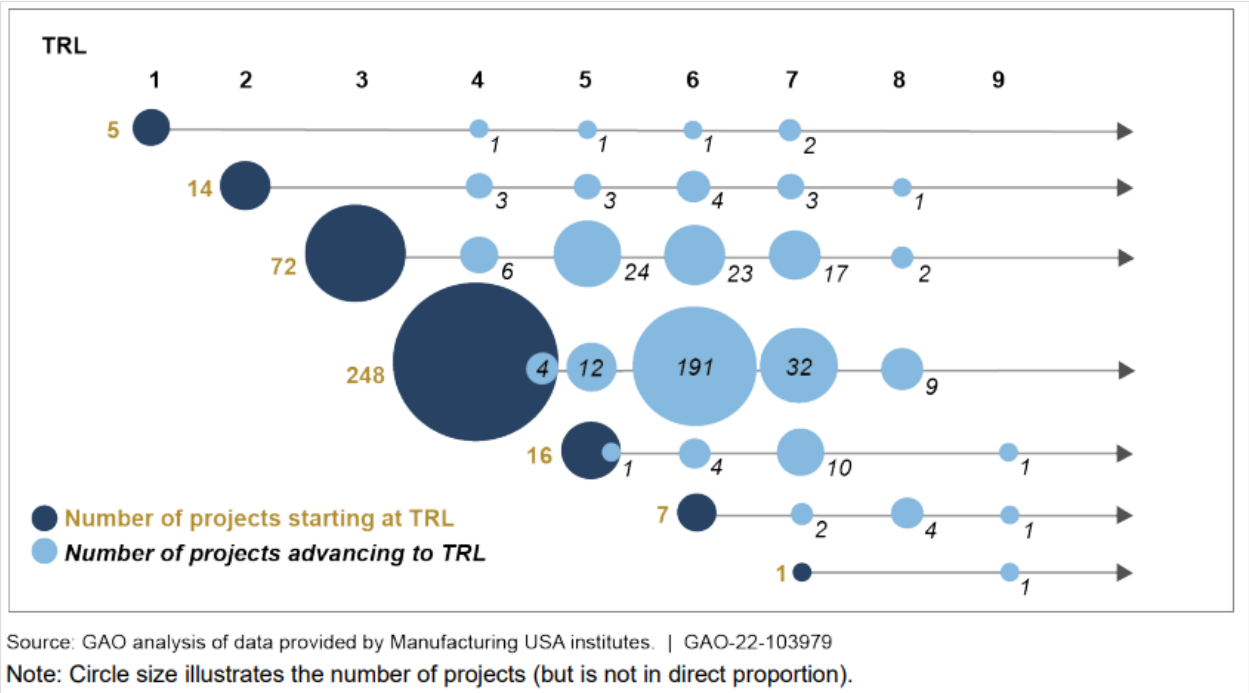

***Figure 1.*** *Microelectronics and Advanced Packaging Technology (MAPT) as a topic for a Microelectronics Manufacturing USA Institute (MMI) to bridge the Lab-to-Fab gap vision*

# Section 1 - Institute Scope

Q1. The Manufacturing USA semiconductor institute program is one component of an $11 billion R&D effort that includes the National Advanced Packaging Manufacturing Program, the National Semiconductor Technology Research Center and the NIST laboratories. The entire R&D program is intended to be interconnected and comprehensive, with no gaps and minimal redundancy, to position the United States for technology and workforce leadership in the semiconductor and microelectronics sector for the long-term prosperity of the nation. Additionally, the Manufacturing USA authorizing statute specifies that new institutes must not substantially duplicate the technology focus of any other Manufacturing USA institute. From your perspective, what role do you envision for new Manufacturing USA semiconductor institutes that will best complement the other R&D investments and remain consistent with the programmatic purposes of Manufacturing USA? Since the Secretary of Commerce may award financial assistance to any existing Manufacturing USA institutes for work relating to semiconductor manufacturing, what role do you envision for existing, federally sponsored Manufacturing USA institutes with respect to semiconductor manufacturing?

The different R&D programs envisioned under the CHIPS Act should together enable a semiconductor ecosystem for a vibrant lab-to-fab transition. Historically, the Manufacturing USA Institutes (M-USA) have been effective by starting projects at the "lab" end of the spectrum and delivering to the "fab" end; most M-USA projects have started at Technology Readiness Levels 3 or 4[2] as shown in Figure 2Error! Reference source not found.. However, since tools for "upstream" activities of chip-package co-design are not readily available, more integration at lower TRLs is necessary for semiconductors. Given this, and given the plans for NSTC and NAPMP, the newly formed M-USAs for semiconductors will be most effective starting at TRLs 2-4 beginning with design/simulation, then transitioning to TRLs 4-5, short of building a prototype system but feeding explicitly and directly into other CHIPS Act R&D programs such as NSTC and NAPMP.

[2] www.gao.gov/assets/gao-22-103979-highlights.pdf




Source: GAO analysis of data provided by Manufacturing USA institutes. | GAO-22-103979

Note: Circle size illustrates the number of projects (but is not in direct proportion).

***Figure 2.*** *Advancement of Technology Readiness Level (TRL) for completed Manufacturing Institute projects as of March 2021*

The role for existing federally sponsored Manufacturing USA institutes would be to directly collaborate with the new Microelectronics Manufacturing USA Institutes (MMI) through joint R&D projects and workforce development programs and inform the new MMI's as they remain focused more specifically on mainstream semiconductor manufacturing (including microelectronics and advanced packaging technology). The current Manufacturing USA institutes that are most related to semiconductor manufacturing include AIM Photonics (for integrated photonics), NextFlex (for flexible electronics) and Power America (for power electronics using wide bandgap semiconductors). We also suggest CESMII (Smart Manufacturing) and ARM (robotics) as cross-cutting institutes. Each of the existing institutes address important topics of emerging microelectronic components and applications, however, they do not directly focus on mainstream developments in semiconductor manufacturing.

In support of collaboration, we recommend that some of the CHIPS Act funding should go to existing manufacturing institutes and dedicated to collaboration with the possible institute(s) established from this RFI. Collaborations could include governance where leaders from existing institutes participate on boards of the new institute(s), in road mapping activities, on proposals and projects, on joint EWD activities, or in joint technology transfers to NSTC and NAPMP.

**Q2.** The technological breadth of innovation in semiconductors and microelectronics is likely larger than can be served by any single Manufacturing USA institute. Therefore, each Manufacturing USA semiconductor institute should have an appropriate scope to ensure that each institute is impactful and does not duplicate efforts of other programs. Historically, institutes in the current network of existing Manufacturing USA institutes have generally been funded for an initial 5 years at $150 million to $600 million, including federal funding and cost-sharing (co-investment) from non-federal partners. What would be the ideal scope and corresponding financial investment from federal and non-federal partners, for a Manufacturing USA semiconductor institute to achieve the needed impact on competitiveness?

Given the need for global competitiveness and onshoring capacity, and to ensure that the new Manufacturing USA semiconductor institute is impactful, it is recommended that a single institute be created through a public-private partnership (PPP) that integrates both microelectronics and advanced packaging technology (MAPT) at a much higher investment level as compared to typical M-USA. To achieve the needed impact on competitiveness, the minimum requirement would be at least $250M/year, with $125M/year federal funding and $125M/year non-federal cost share. We anticipate cost share will increase in subsequent years but would begin with a 1:1 ratio. Since the global semiconductor manufacturing industry revenue was $560B in 2021[3] with $1,065 billion[4] projected by 2030, we recommend the size of the institute follow a similar growth trajectory.

This investment has impact across multiple end markets. According to Deloitte, the chip shortage in the past two years resulted in revenue losses of more than $500 billion worldwide between the semiconductor and its customer industries, with lost auto sales of more than $210 billion in 2021 alone.[5] A new M-USA institute of an appropriate magnitude and scope would help to reverse the impact of the recent shortage and further reduce the risk of future recurrences.

Currently, high costs as well as lack of in-house talent restrict access to electronic design and analysis (EDA) tools, modeling, technology customization, metrology tools, product qualification, and reliability assessment for small and medium-sized enterprises. The above activities are critical to create an open microelectronics and advanced packaging technology lab-to-fab ecosystem in the US. However, these activities are not part of existing Manufacturing USA Institutes and therefore necessitate a broader scope and higher funding levels for the planned institutes.

[3] www.semiconductors.org/wp-content/uploads/2022/11/SIA_State-of-Industry-Report_2022.pdf
[4] www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry
[5] https://www.reuters.com/business/autos-transportation/automakers-chip-firms-differ-when-semiconductor-shortage-will-abate-2022-02-04/#:~:text=Latest%20Updates&text=The%20chip%20shortage%20will%20cost,consultant%20AlixPartners%20estimated%20in%20September

**Q3.** Potential technology areas of focus that could be addressed by the Manufacturing USA semiconductor institutes to complement the National Advanced Packaging Manufacturing Program and the National Semiconductor Technology Research Center in Question 1 are listed below. What are your thoughts on the appropriateness of each for the scope of work for a Manufacturing USA semiconductor institute? What other topics should be included in the scope of an institute?

- Chip-package architectures and co-design of integrated circuits and advanced packaging. May include artificial intelligence, security, test methodologies, etc.
- Technologies to increase the microelectronics manufacturing productivity of American workers, lower costs and offset the drastic shortfall of skilled workers.
- Assembly and Test metrologies to develop new analytical equipment and analysis capabilities based upon standards.
- Coding and system software with novel computing paradigms and architectures, including chiplet compatibility with earlier generations.
- Integration of security into packaging, interposers and/or substrates.
- High Density Interposers and substrates, incorporating new materials and designs.
- Chiplet-enabled trusted packaging facilities that obviate the need for trusted foundries.
- New materials, such as glass for substrates, or compound semiconductors.
- Environmental Sustainability for semiconductor manufacturing.
- Analog and Gigahertz Technology materials and metrology, enabling beyond 5G, the Industrial Internet of Things and Industry 4.0.
- Performance and Process Modeling and Metrology

The topics proposed above are highly appropriate for the scope of MMI R&D topics, however additional technical topics related to semiconductor manufacturing technology are necessary. The technical topics included within the scope of the institute(s) should be guided by the community consensus, NIST-sponsored Manufacturing and Advanced Packaging Technology (MAPT) roadmap which includes contributions from over 90 organizations within the semiconductor ecosystem. The initial reports have been provided to NIST and a preliminary public release is expected in Q1 2023.

Beyond using the MAPT Roadmap as a guide, the scope of the institute should include the full stack of R&D from devices, structures, and materials through circuits, architectures, and algorithms. More specific technologies include:

- Digital Processing
- Analog/ Mixed Signal Processing
- Micro(nano)-electromechanical systems MEMS/NEMS and sensors
- Device processing and manufacturing yield estimation
- Integrating thermal solutions with chip stacks
- Reliability assessment of complex semiconductor devices and advanced microelectronic packages
- Chiplet interconnection standards

It is imperative that the new Manufacturing USA semiconductor institute integrate both microelectronic and advanced packaging topics, rather than focusing on one or several stand-alone technical areas. The 2030 SRC Decadal Plan for Semiconductors[6] describes the need for benchmarking advances needed in both microelectronics and advanced packaging technology to drive and deliver the holistic needs of systems. The critical need for such co-design and co-integration between microelectronics and advanced packaging was projected, in-part, by Gordon Moore in his famous paper, *"Cramming More Components onto Integrated Circuits"* (1965), which forms the basis of "Moore's Law." He states that "The total cost of making a particular system function must be minimized … [at some point] *It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected*. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically." He refers to this as the "day of reckoning."

Today, the 'day of reckoning' has arrived and there is no critical mass in the US in this new era of Moore's Law – this is a key opportunity for the new Manufacturing USA semiconductor institute. Where monolithic integration forms all circuit functions on a single common semiconductor (at the wafer scale), heterogenous integration enables the concatenation of 'chiplets' of various functionalities (logic, I/O, memory, power conversion, passives, photonics, mm-wave, etc.) and materials in a manner that mimics/exceeds monolithic-like performance and utilizes advanced off-chip '2.5D' and '3D' interconnects and packaging to provide flexibility in fabrication and design, improved scalability, reduced development time, and reduced cost.

This approach is becoming accepted commercially; Figure 3 below gives a brief snapshot of the various emerging advanced packaging concepts in this new era of Moore's Law. While these

[6] www.src.org/about/decadal-plan/

emerging packaging technologies vary in approach, they all seek to blur the boundary between on-chip and off-chip interconnect densities for power and performance considerations and train the workforce to adopt this evolving mindset.

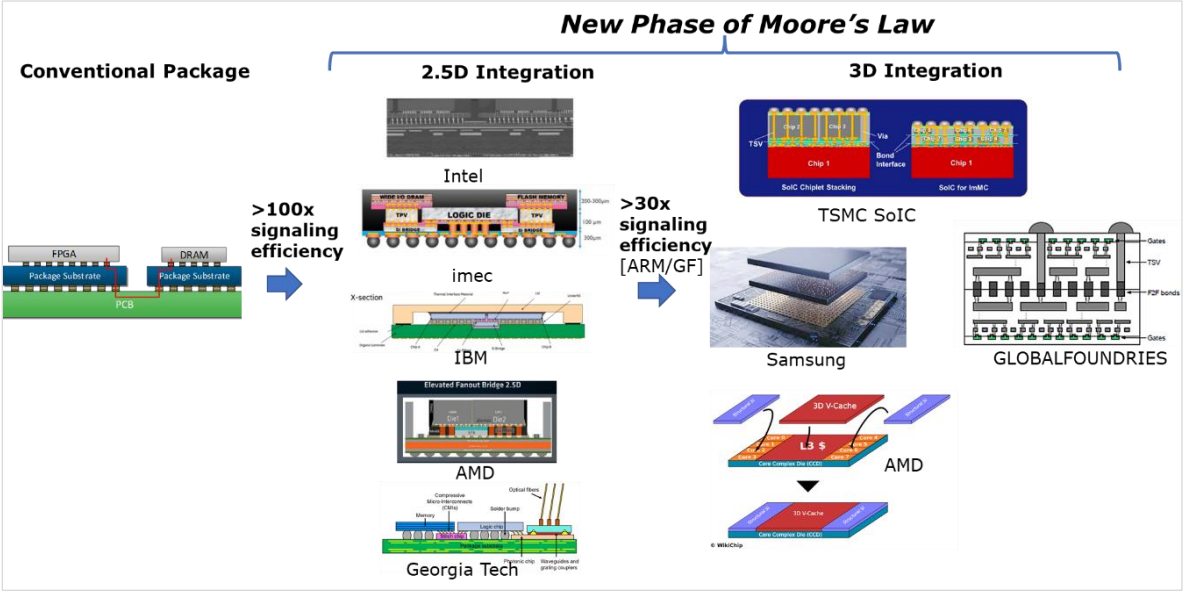



***Figure 3.*** *Snapshot of the various emerging advanced packaging concepts in the new era of Moore's Law*

## **Q4.** What criteria should be used to select technology focus areas in delineating the scope for a Manufacturing USA institute focused on semiconductor manufacturing?

The criteria for selecting technology focus areas must be driven by industry, especially those with significant domestic manufacturing capacity, with input from academia and government. The technology selection should be consensus-driven and be built on a foundation from existing and ongoing roadmaps. The selection criteria must also include the feasibility of the technology to impact the goals of the MMI, NIST, and the CHIPS Act, supporting a robust manufacturing infrastructure that can be sustained well beyond the 5-year target funding from government while reducing manufacturing supply chain risks. Additional criteria should include:

- Impact that the technology can have on bringing underrepresented communities and geographic regions into the industry
- TRL/MLR aligned with the M-USA institute model, which is typically 3- 5[7]
- Complementary to adjacent CHIPS Act programs including NSTC, NAPMP, DOD Commons, and NIST metrology

[7] www.gao.gov/assets/gao-22-103979-highlights.pdf

- Ability to co-optimize microelectronics technology with advanced packaging technology to make the sum better than each individual
- Strong emphasis on equitable drivers for semiconductor workforce development across all levels of post-secondary education levels

Q5. What technology focus areas that meet the criteria suggested in Question 4 above would you be willing to co-invest in?

SRC is a crossroads of collaboration between technology companies, academia, government agencies, and other participants in the semiconductor ecosystem. With 27 member companies supporting US manufacturing, partnering with more than 100 universities and multiple government agencies, SRC manages several research programs with a combined 55 research topics and more than 500 research projects carried out by over 1,200 SRC-sponsored students annually. For the Manufacturing USA Institute, SRC and its members would co-invest in the technical topics illustrated in **Figure 4** below to ensure comprehensive R&D and impact. These topic areas are aligned with the NIST Microelectronics and Advanced Packaging Technology Roadmap (in progress), and industry is currently funding these topics through active SRC research programs now.

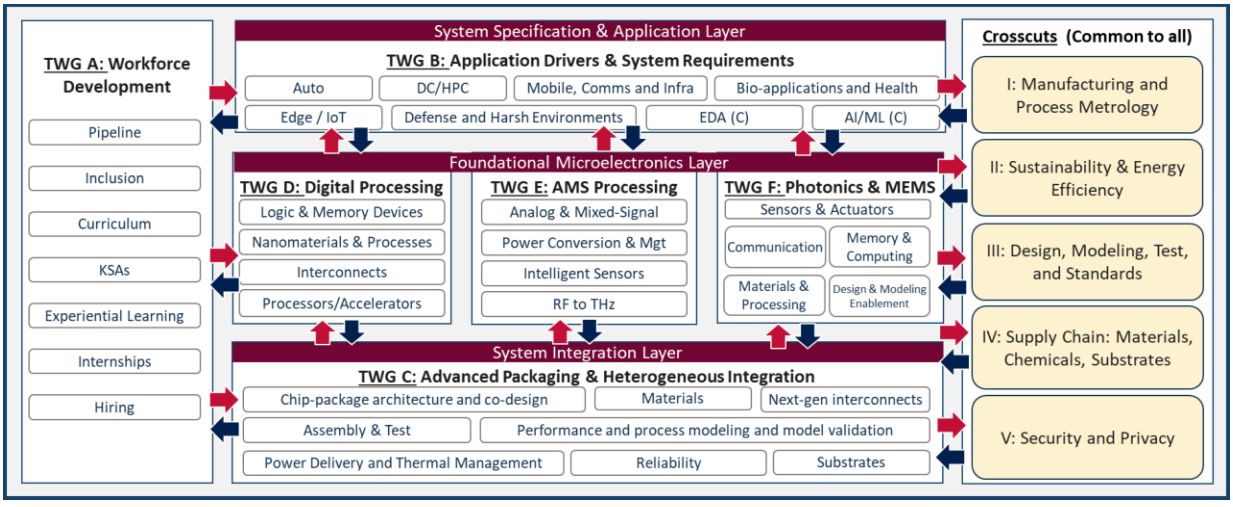
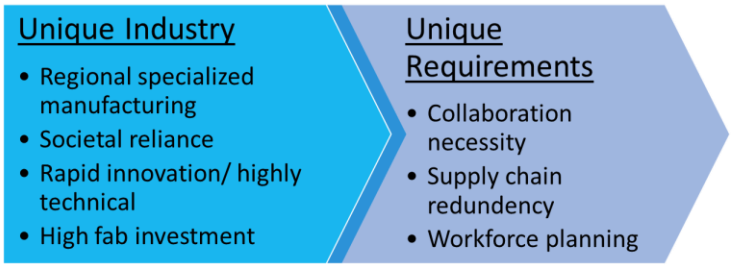



*Figure 4. Suggested technology structure of a Manufacturing USA institute focused on semiconductor manufacturing by adopting learnings from NIST- sponsored MAPT Roadmap, with contributions from over 90 organizations in the semiconductor ecosystem*

# Section 2: Institute Structure and Governance

Q6. Existing Manufacturing USA institutes were launched and operate in alignment with the design principles published in 2012 as the *National Network for Manufacturing Innovation: A Preliminary Design*. Are there any unique considerations for the semiconductor and microelectronics sector that may require modifications to the conventional design for any Manufacturing USA semiconductor institutes under consideration?

**UNIQUENESS OF THE INDUSTRY**




The semiconductor industry differs from many other manufacturing industries in four distinct ways: 1) regional specialized manufacturing, 2) societal reliance; 3) rapid innovation cycles of high technology; and 4) extremely high manufacturing facility costs. Here is how each of these four attributes make the industry unique:

### 1) Regional Specialized Manufacturing

Over the past several decades, the semiconductor industry has changed the way we work, play, and connect, while enabling trillions of dollars in economic prosperity and transforming national security. However, during these decades, the industry fractured into specialized parts of the collective manufacturing process (

Figure *5*), each of which is highly sophisticated and not readily duplicated because of specialized manufacturing and IP. While each of these specializations has different economic and risk characteristics, together they deliver a system that has enabled massive industrial growth and yields a global supply chain that is highly optimized to convert silicon ingots into integrated circuits for many industries and consumer applications.

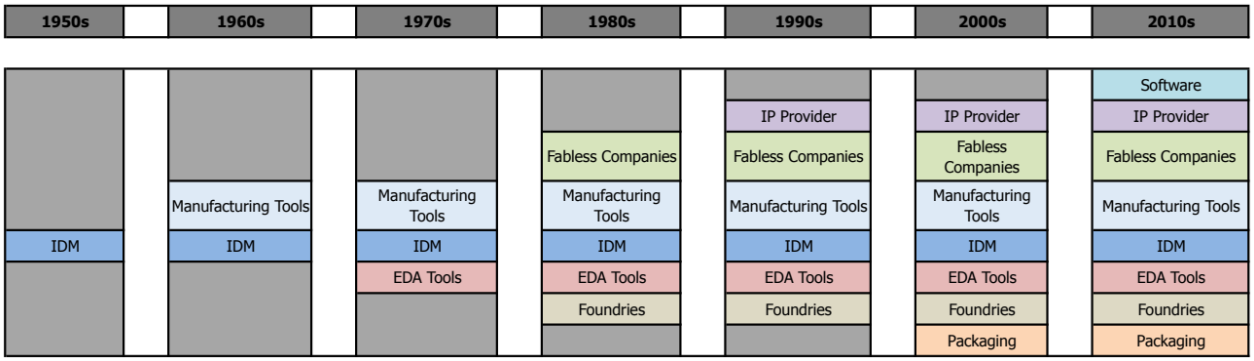


*Figure 5. Functional evolution of the Semiconductor Ecosystem (1950s-2010s) into specialized elements of the supply chain*[8]

As the semiconductor industry evolved into these specialized elements, geographic regions emerged as hubs of the supply chain (Figure 6). This regional specialization has enabled global economic growth for over 40 years and the continuation of Moore's Law well beyond what a single actor, alliance, or region could have accomplished.

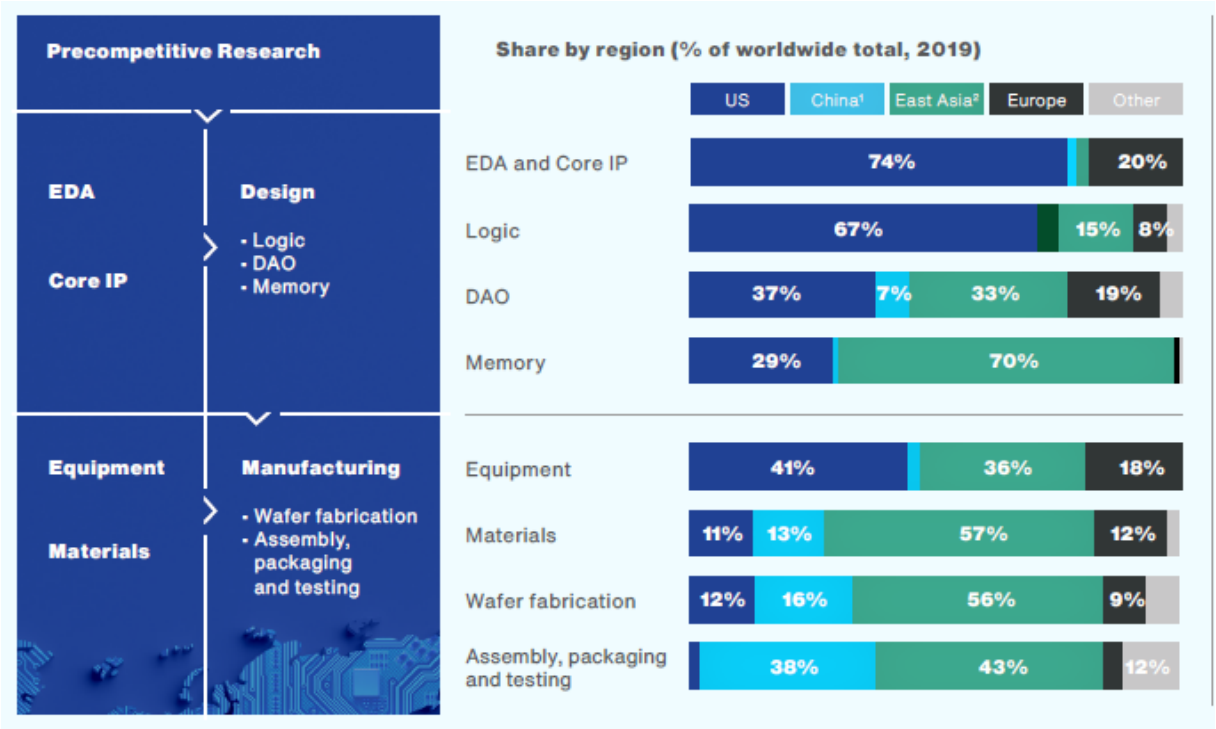



*Figure 6. An Example of the Semiconductor Global Supply Chain and Its Specialized Regions*[9]

Although this regional specialization enabled global economic prosperity, it has resulted in excessive risk and growing economic dependence on foreign sources, excessive risk to national security, and a lack of visibility into global demand and shortages for manufacturing (Figure 7).

[8] www.semiconductors.org/wp-content/uploads/2018/06/SIA-Beyond-Borders-Report-FINAL-June-7.pdf
[9] www.semiconductors.org/wp-content/uploads/2021/05/BCG-x-SIA-Strengthening-the-Global-Semiconductor-Value-Chain-April-2021_1.pdf

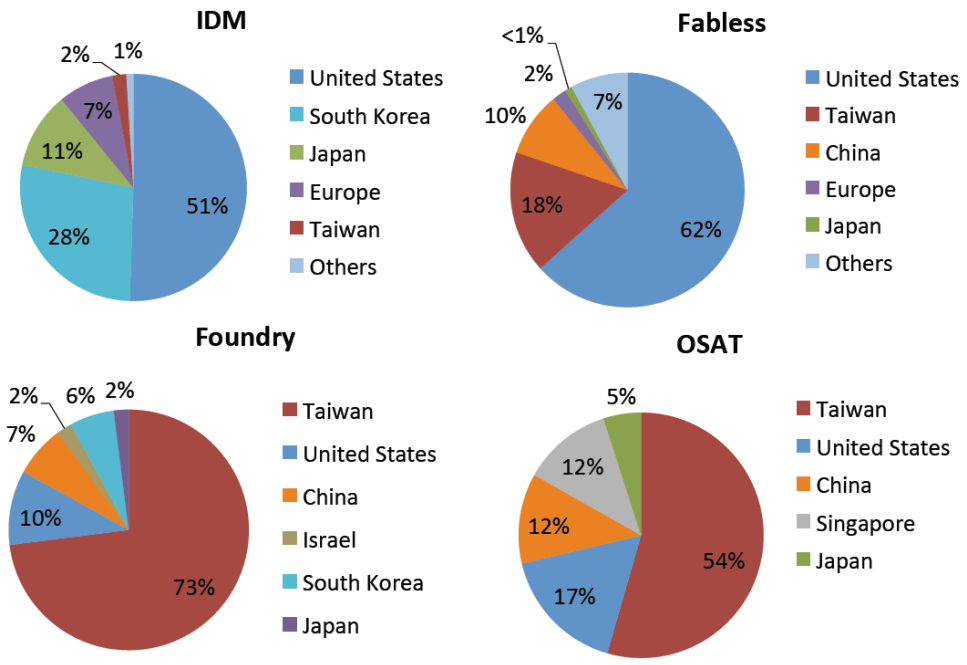



*Figure 7. Internationalization of the Semiconductor Value Chain (% of Total Revenue, 2015)*[10]

Many vulnerabilities exist throughout the manufacturing supply chain, which amount to a critical threat to National Security. Of particular concern are the risks associated with Outsourced Semiconductor Assembly and Test (OSAT). OSAT's are an important part of the supply chain and are particularly vulnerable because they are often the last step before integration into a system. For example, bad actors can target OSAT processing by inserting trojans into packages, resulting in great risk to national security.

A new institute will create domestic advanced packaging technology (APT) R&D capabilities, leading to domestic manufacturing capabilities and a more robust and secure supply chain. This APT infrastructure needs to be tightly coupled and integrated with microelectronics to co-design between chips and packaging.

## 2) Societal Reliance: "Chips are the foundation of the modern world"

Society relies on semiconductors. They have become essential to our quality of life whether navigating to a soccer game, communicating with loved ones, making payments, or managing workflows.

Semiconductor chips are a critical ingredient to the economy for both manufacturing and non-manufacturing segments. As Donna Dubinsky, Senior Counselor to the Secretary for CHIPS

[10] https://www.semiconductors.org/wp-content/uploads/2018/06/SIA-Beyond-Borders-Report-FINAL-June-7.pdf

Implementation, stated in the *CHIPS for America Incentives Program* webinar on September 29, 2022: "Chips are the foundation of the modern world." Manufacturing for most industries relies on a steady, reliable supply of trusted semiconductors. Any disruption in chip supply can have dramatic effects on manufacturing across many industries and on the economy, as was felt during the pandemic. Semiconductors are the building blocks of many other non-manufacturing industries that cease to function without them. Examples include:


- Automotive
- Banking and finance
- National infrastructure spanning GPS, the power grid, communications and data networks, transportation networks, etc.
- Aerospace, Defense, and weapons systems
- Healthcare

### 3) Rapid Innovation/ Highly Technical

The technical capabilities of the semiconductor industry are unmatched. Moore's Law has provided the industry with a steady cadence of performance gains such that the number of transistors on a chip has doubled every two years for about half a century. Further, the number of transistors manufactured is staggering at a cumulative total of 13 sextillion ($1.3\times10^{22}$) manufactured worldwide between 1960 and 2018[11]. That is roughly one transistor for every grain of sand on earth. Some transistors are just a few atoms wide, while the range of power management for transistors varies from nano-watts to kilowatts. This technology and innovation are only possible because of the high R&D intensity (R&D expenditures/Revenue) throughout the industry. The only industry that surpasses semiconductor R&D intensity is Pharma & Biotech[12].

### 4) High cost of capital expenditures for manufacturing

Manufacturing semiconductors is a high capital expenditure (capex) endeavor because of the high cost of specialized equipment and the cost of controlled environment requirements in which to

[11] https://computerhistory.org/blog/13-sextillion-counting-the-long-winding-road-to-the-most-frequently-manufactured-human-artifact-in-history/?key=13-sextillion-counting-the-long-winding-road-to-the-most-frequently-manufactured-human-artifact-in-history
[12] www.semiconductors.org/wp-content/uploads/2022/11/SIA_State-of-Industry-Report_2022.pdf

manufacture chips. Typically, the industry spends about 20% of revenue on capex, with construction of a single fabrication facility costing up to $20B[13].

**SPECIAL CONSIDERATIONS**

Due to the unique attributes mentioned above, there are primarily 3 special considerations for creating and operating a Microelectronics Manufacturing USA Institute (MMI). These include: 1) the necessity to collaborate, 2) the need for supply chain redundancies, and 3) considerations for workforce development planning. Each of these is discussed in the following three sections:

### 1) Collaboration Necessity

There will be a large number of participants, partners, and members all working together. Critical collaboration would need to happen between all of the CHIPS Act R&D programs including NIST Metrology, MMI, NSTC, and NAPMP, as well as the Workforce and Education Fund, the DOD Commons, and the International Technology Security fund. Only by working together can the objectives of CHIPS Act be met. Designing and creating these programs and corresponding PPP's accordingly will ensure no gaps with minimal overlaps, and best leverage the funds provided by Congress to build a complete innovation pipeline with seamless integration. This will also be important to avoid market failure between Proof of Concepts created in government and university labs, and the development, scaling, and manufacturing capabilities of the industry.

It is highly important for the MMI to interact with other Manufacturing USA institutes within the network, and preferably collaborate across institutes on research topics. Not only would this strengthen the performance of both institutes, but it would enhance the performance of the M-USA network.

Collaboration between different scientific disciplines is also needed. Interdisciplinary collaboration across many technical fields such as Materials Science, Physics, Electrical Engineering, Mechanical Engineering, Chemistry, Computer Science, and more have been the requisite recipe for innovation success in the industry and must be continued through this institute.

### International Collaboration

The institute will need to include international partners from the US and ally countries for any comprehensive solution, thereby creating "democracy chips" (chips manufactured in democratic countries) to ensure global resources are contributing to the CHIPS Act objectives. This can be a

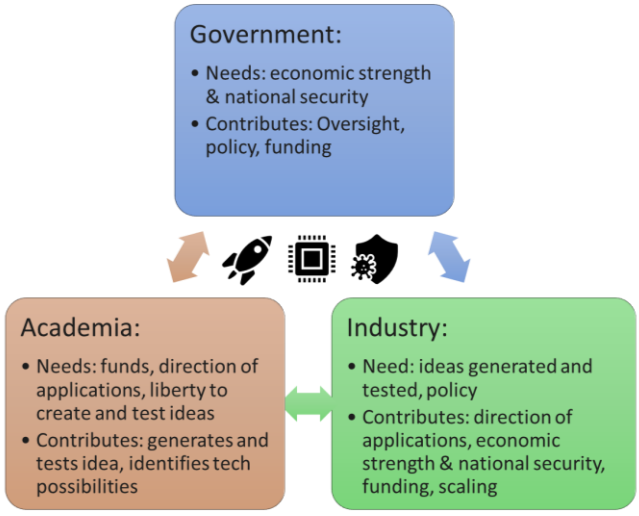
[13] www.semiconductors.org/wp-content/uploads/2020/09/Government-Incentives-and-US-Competitiveness-in-Semiconductor-Manufacturing-Sep-2020.pdf

challenge because, as an international industry, countries that are otherwise adversaries rely on one another to support their respective economies.

For example, China is often perceived as a political adversary of the US. Yet China relies on sourcing semiconductors designed in the US and produced in Taiwan. The US, and our global society at large, are dependent on China to turn those semiconductors into finished products. For security reasons, it is important that the US does not sell state-of-the-art semiconductors to China that could potentially be integrated into weapons systems used against the US and allies.

Industry - Academia - Government Collaboration

The US, along with like-minded nations, have demonstrated the ability to achieve monumental results when government, industry, and academia work together. Historical examples of these monumental achievements include the development and widespread use of vaccines, the first moon landing, and the creation of the semiconductor industry and internet. In order to achieve success on a similar scale in the semiconductor industry, each of those three entities must play a unique role to ensure the relationship is symbiotic:




a) ***Government*** should initiate creation of the institute, but not be the dominant sponsor in perpetuity. Instead, government sponsorship should diminish after the start-up period. If the institute cannot operate primarily through industry sponsorship, then it is not properly serving the community. Although the government should not generally engage in long-term research agendas, signals of long-term support should be provided by government to ensure industry participation. Government should financially support risk that is too high for industry to pay for alone. Government needs to convince companies investing in the institute that these companies' commitments of human and financial capital will not be abandoned by their government partners in a few years.

b) ***Industry*** should lead the technical direction of the institute because they provide critical knowledge about what technologies the markets will support and what

technologies can be scaled. This position allows industry to best determine which technologies should advance throughout the innovation pipeline. They also provide important insight into past commercial failures - the details of which may not be known to government or academia.

c) *Academia* should be the driving force for creating and testing new technologies that will be matured through the innovation pipeline. Their liberty to create and test new ideas without the burden of meeting quarterly financials must be protected, allowing them to explore new vectors, understand the fundamentals of new innovations, and find new pathways. Further, it will be academia that leads the effort of workforce development.

## 2) Supply Chain Redundancy and Resiliency is needed

Without a complete supply chain, domestic manufacturers are susceptible to failures of which the US is not in control. The global supply chain has historically provided US companies with access to the latest technologies at fair cost and reliable delivery. However, there are increasing risks posed by geopolitical conflict, dramatic weather events, regional economic instabilities, and, most recently, pandemics. These risks threaten the supply chain's stability, and in turn, US economic and national security. Specifically, although US IDM and Fabless/Design companies account for over 50% of the revenue in the semiconductor industry, much of the manufacturing capacity is overseas. This has led to a reduction in US manufacturing capacity from 37% in 1990 to 12% in 2020. Countering this, Samsung and TSMC's growing commitment to building semiconductor manufacturing facilities in the US is a welcomed source of stability.

Each link of the semiconductor supply chain has few participants in niche areas. These are often defined by companies or by regions. For example, ASML dominates lithography equipment; design software is dominated by 3 companies; OSAT is dominated in SE Asia. This creates narrow pinch points throughout the supply chain.

When designing solutions for the domestic semiconductor industry to address supply chain risk mitigation, it is important to have some domestic capability for every step of the supply chain. Unlike other industries that can trade one material or component for another (although sometimes at higher cost) and still function correctly, the semiconductor industry is highly specialized resulting in few to no alternatives to serve as reinforcements of the supply chain.

To further reduce supply chain manufacturing risk in an economical way, the institute should identify adjacent industries that have manufacturing capabilities that can be repurposed with low

barriers to support the semiconductor industry if the supply of critical materials is jeopardized. This is especially true for chemicals and materials, which are generally agnostic to the end application, as compared to integrated systems which are more specific to the end application. For example, the robust US chemical industry could support the semiconductor industry by repurposing resources towards semiconductor-specific needs in the event of an international semiconductor supply chain crisis.

### 3) Workforce planning is needed

There are **four main areas** that must be considered in order to bolster the semiconductor workforce: 1) education and training, 2) geographic challenges, 3) diversity and inclusion, and 4) talent attraction.

**Education and Training** - The semiconductor workforce is unique in that it requires extensive use of MS and PhD educated workers that support the high R&D intensity to develop, support, and optimize the next generation of manufacturing. Compared to other manufacturing, the semiconductor industry relies on a workforce with about twice as many bachelor's degrees and advanced degrees **(Figure 8)**. To support this, access and retention of both US and foreign-born talent is critical to the industry's workforce needs[14].

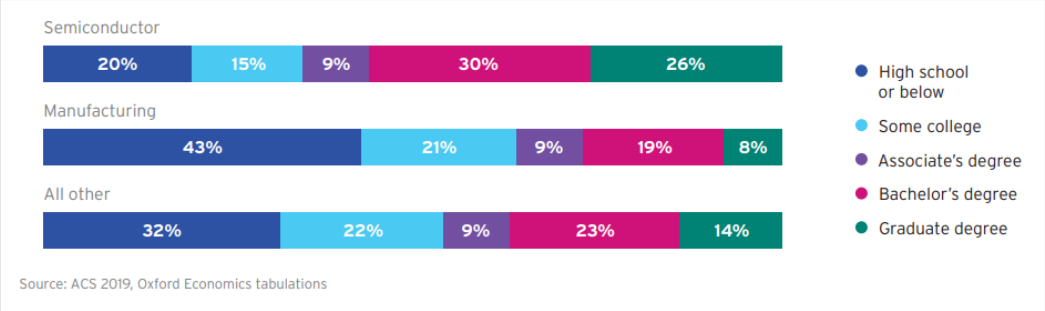



***Figure 8.*** *Educational attainment in the semiconductor industry*

**Geographic Challenges** - Equipment operators and technicians with specialty skills and training are also critical to the industry. In general, these technicians look for work in factories located in the same region in which they completed training and do not tend to relocate. Conversely, semiconductor manufacturing workforce with graduate degrees are more apt to move to a different region or even a different country to find work.

**Diversity and Inclusion** - Historically, the semiconductor industry represents a homogenous workforce of predominantly men that are Asian and Caucasian **(Figure 9)**, where men make up 75-

[14] www.semiconductors.org/wp-content/uploads/2021/05/SIA-Impact_May2021-FINAL-May-19-2021_2.pdf

90% of the industry workforce[15]. A truly resilient workforce needs to be diverse and inclusive of all ideas and capabilities, including underrepresented communities.

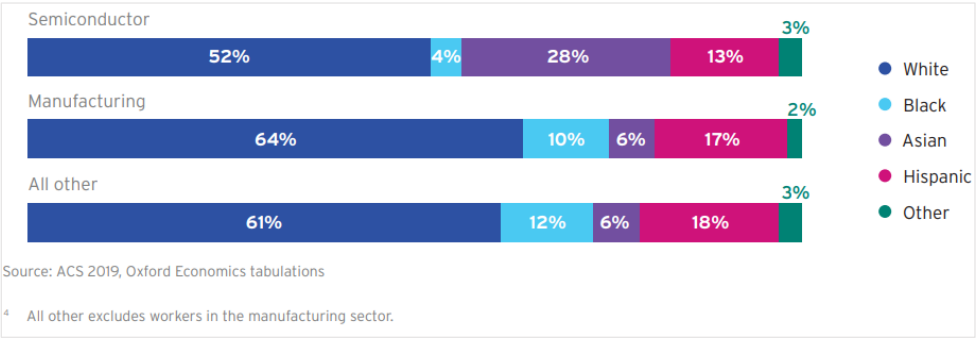



*Figure 9. Race and ethnicity profile*

**Talent attraction:** To supply enough workers for the industry there must be programs to attract High School graduates into the field. This could require a span of approaches including engineering competitions, hands-on workshops, 'educating the influencers' programs for High School math and science teachers as well as guidance counselors, and engineering career days.

Q7. Semiconductor R&D and manufacturing cover substantial technical breadth.

A) What business models or best practices should be employed by a Manufacturing USA semiconductor institute to support U.S. leadership and effectively manage emerging technologies to support commercialization?
B) What advantages or disadvantages would there be to one "super-sized" Manufacturing USA semiconductor institute that would cover the technology sector broadly?
C) Since Congress authorized the NIST Director to establish up to three institutes, what advantages or disadvantages would there be for multiple Manufacturing USA semiconductor institutes each with a smaller scope focused on a specific technology area?
D) How would one Manufacturing USA semiconductor institute or multiple institutes structure relationships with other significant partners to spur collaborative work?

### A) Business models and best practices

We acknowledge the excellent best practices and review work performed as required by the Revitalize American Manufacturing and Innovation (RAMI) Act of 2014. Manufacturing USA was created to improve the competitiveness of US manufacturing by accelerating innovation and implementation of advanced manufacturing capabilities. Each institute creates the necessary

[15] www.gsaglobal.org/wp-content/uploads/2020/05/BRIEF-GSA-Women-in-the-Semiconductor-Industry-Survey-Results-2019.pdf

focus and provides the state-of-the-art facilities needed to allow collaborative, pre-competitive development of promising technologies. An institute provides workforce education and training in advanced manufacturing. It also promotes the creation of a stable and sustainable innovation ecosystem for advanced manufacturing. We also acknowledge the National Academies report "Manufacturing USA Revisited: Securing Advanced Manufacturing in the United States - A Workshop.[16]"

While reading these reports and leveraging SRC and other collaboration models, we recommend the following attributes be included in an MMI governance and business model:

1) The organizations creating, operating, and managing the institute should have the authority to make timely decisions, yet still be accountable and transparent.
2) The institute must be flexible and adaptable to incorporate new insights for optimization. That is, as the organization begins to operate, there will be new realizations of what works and what does not. It will be important to incorporate these findings to refine the operational model.
3) The institute must require rotation of leadership to welcome fresh perspectives from organizations and activate the larger community. For example, Board of Directors chair, Technology Advisory Board chair, Government Advisory Board, etc.
4) The institute must produce specific, measurable, short- and long-term goals with accountability to a management oversight board to ensure performance. To support this, the governance must:
    a) Be a trusted, credible, guide for the industry
    b) Use transparency, data-driven decisions, and consensus
    c) Drive collaboration, consensus, and cooperation as imperatives
    d) Operate under and OTA authority with government
5) The institute must focus on collaboratively funded R&D. This was discussed extensively in the response to Question 6.
    a) User facilities that are available to all members and mapped to their interests
    b) IP structures that enable collaboration and investment
        i) Share IP so partners can collaborate together
        ii) Protected/ limited access IP allows for greater financial investments by industry members
        iii) Encourage inclusion and protection of background IP

[16] www.nationalacademies.org/our-work/manufacturing-usa-securing-advanced-manufacturing-in-the-united-states-a-workshop

6) The institute must include of all parts of the ecosystem, including:
    a) all aspects of supply chain - from materials suppliers through systems integrators
    b) industry, academia, government, trade organizations, etc.
    c) start-ups through industry titans from the US and like-minded nations
    d) US higher education - from trade schools and community colleges through tier 1 research universities, minority-serving institutions, veteran training, reskill/ upskilling; geographic diversity and underserved communities
    e) span the full stack - from materials through packaging, applications, and hardware/ software codesign

*Technology Transfer*

Critical to meeting the objectives of the CHIPS Act strategy and the M-USA institute(s) is the need to ensure technology transfers from research, through the innovation pipeline, to manufacturing using a stage-gate methodology to increasingly invest in maturing the most promising technologies. Developing technology but not transferring it to industry can be an enormous missed opportunity for supporting national interests. As such, the institute must use best practices for ensuring that technologies become useful. To do this, a full portfolio of approaches must be used across different levels of technology maturity and technology type (materials, design, software, etc.) to ensure it remains on a path to market. Several methods have proven highly effective such as DARPA's Embedded Entrepreneurship Initiative and SRC's industry liaisons.

Start-ups can be a rich resource for transferring technology into manufacturing. To benefit from this the institute should support concepts employed by Silicon Catalyst and transition them into a national resource available at the Institute.

The broad goal of this innovation pipeline is to create new technology, mature that technology, and manufacture it to strengthen the US economy, national security, and society as a whole. Here are three examples of how the technology pipeline - from academic labs to manufacturing - would work. We recommend that each of these be pursued in appropriate proportions:

1) Transfer technology from the institute directly into commercial members using best practices that are proven to work as mentioned above.
2) Transfer technology from the institute to prototyping and development facilities, such as the Coalitions of Excellence (COE's) associated with the NSTC and/or NAPMP for maturation before transferring into industry.

3) Transfer technology from the institute to start-ups for maturation and ultimately for manufacturing, either directly by the startup or through acquisition of the start-up by a manufacturing company.

*General best practices*

To support the financial needs of the MMI, and following along with others' best practices, it will be helpful to allow the institute to support privately funded initiatives using institute resources for a fee.

## B) Advantages of a super-sized MMI

*[Note: some portions of this response are restated from Question 3 responses]*

It is imperative that the new Manufacturing USA microelectronics institute integrate both microelectronic and advanced packaging topics, rather than focusing on one or several stand-alone technical areas. The 2030 SRC Decadal Plan for Semiconductors[17] describes the need for benchmarking advances needed in both microelectronics and advanced packaging technology to drive and deliver the holistic needs of systems. Further, the critical need for such co-design and co-integration between microelectronics and advanced packaging was projected, in-part, by Gordon Moore in his famous paper, *"Cramming More Components onto Integrated Circuit"* (1965), which forms the basis of "Moore's Law." He states that "The total cost of making a particular system function must be minimized … [at some point] *It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected*. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically." He refers to this as the "day of reckoning."

Today, the 'day of reckoning' has arrived and there is no critical mass in the US in this new era of Moore's Law – this is a key opportunity for the new Manufacturing USA semiconductor institute. Where monolithic integration forms all circuit functions on a single common semiconductor (at the wafer scale), heterogenous integration enables the concatenation of 'chiplets' of various functionalities (logic, I/O, memory, power conversion, passives, photonics, mm-wave, etc.) and materials in a manner that mimics/exceeds monolithic-like performance and utilizing advanced off-chip '2.5D' and '3D' interconnects and packaging to provide flexibility in fabrication and design, improved scalability, reduced development time, and reduced cost.

[17] www.src.org/about/decadal-plan/

This approach is becoming accepted commercially; **Figure 10** below gives a brief snapshot of the various emerging advanced packaging concepts in this new era of Moore's Law. While these emerging packaging technologies vary in approach, they all seek to blur the boundary between on-chip and off-chip interconnect densities for power and performance considerations. As such, it is critical that the new Manufacturing USA semiconductor institute combines microelectronics and advanced packaging.

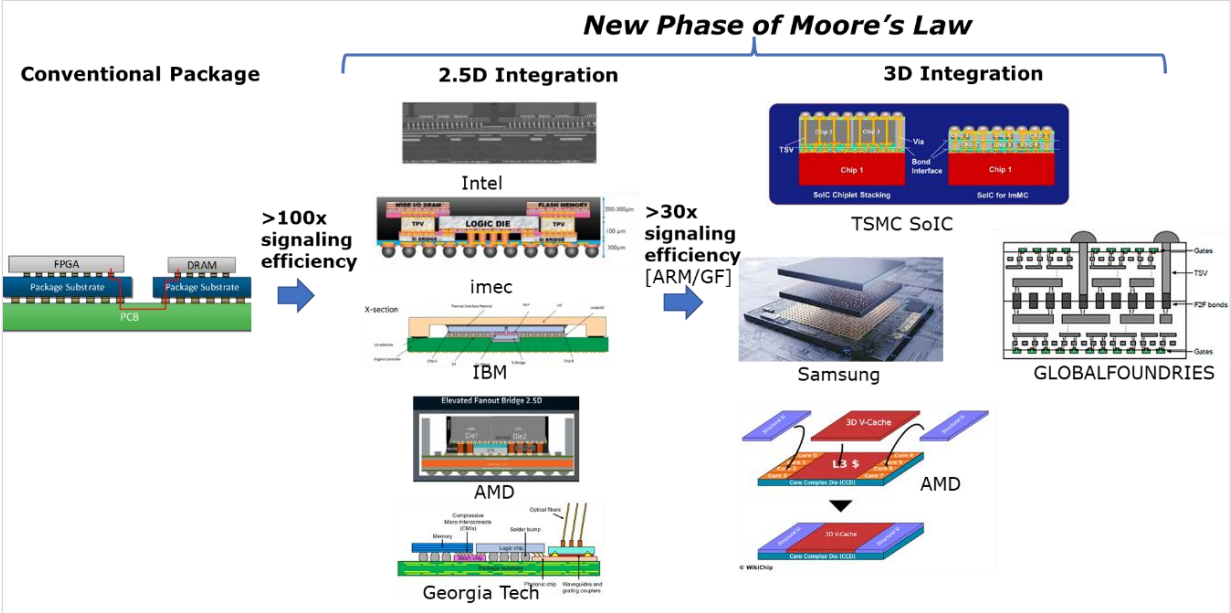
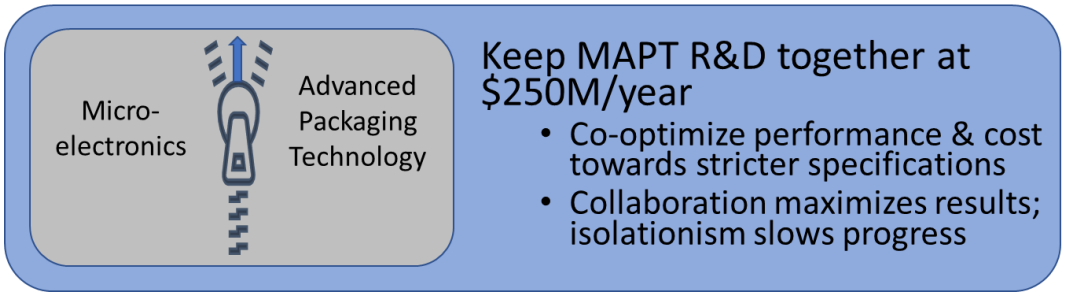
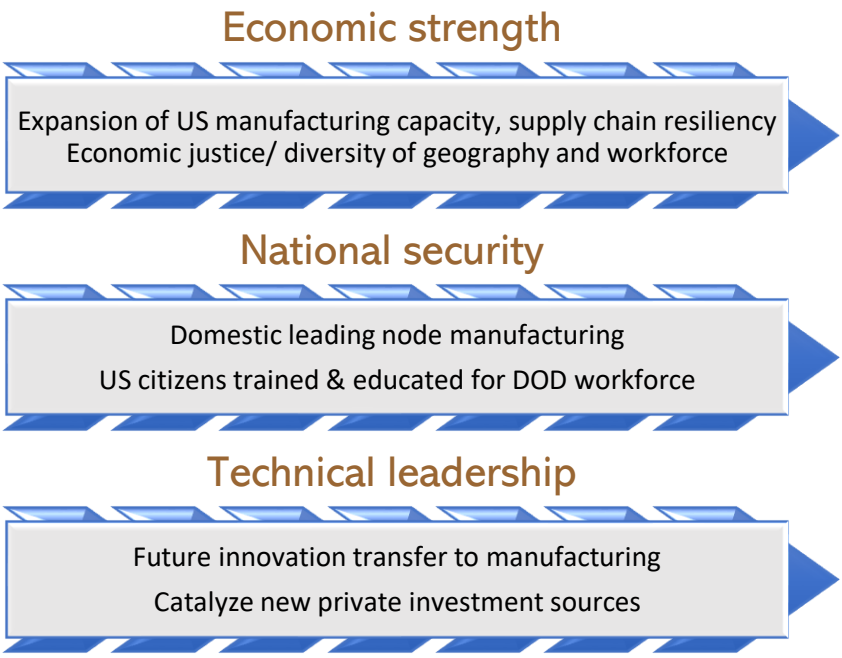



***Figure 10.*** *Snapshot of the various emerging advanced packaging concepts in the new era of Moore's Law*

Given the magnitude of the industry and global impact needed and the breadth of technologies, we recommend one 'super-sized' institute that covers technical areas associated with Microelectronics and Advanced Packaging Technology (MAPT) along with a possible second, and separate, independent institute, which is of standard size, covering technical areas of Virtualization, Visualization, and Automation (VVA) especially for fab construction and operation.



Creating and operating a super-sized MMI based on MAPT would advance research and commercialization of semiconductor manufacturing technology more competitively, thereby have a direct impact on:




***One Super-Sized institute to build domestic multi-dimensional Microelectronics and Advanced Packaging Technology (MAPT) Infrastructure:*** The US microelectronics infrastructure excels at basic, and early-stage applied research. While this is true for microelectronics, there is a limited infrastructure for advanced packaging technology R&D domestically, including 2.5/3D stacking, heterogeneous integration, chiplet design, etc. We recommend that the institute include the continuation of nurturing the semiconductor infrastructure for R&D while building the R&D infrastructure for Advanced Packaging Technologies 10-100X larger than it is today. As 2D geometric scaling runs out of atoms for transistors in the coming years, the next wave of cost/performance gains will come from 3D integrated circuits (3DIC) through both monolithic and heterogeneous integration with increased reliance on advanced packaging technologies. These technologies will drive the continuation of Moore's Law technology and economic advancements in the coming years. Since no country currently has an extensive advantage in this 3DIC field, the opportunity is ripe for the US to take leadership and reap the rewards in the following decade for Microelectronics and Advanced Packaging Technology (MAPT).

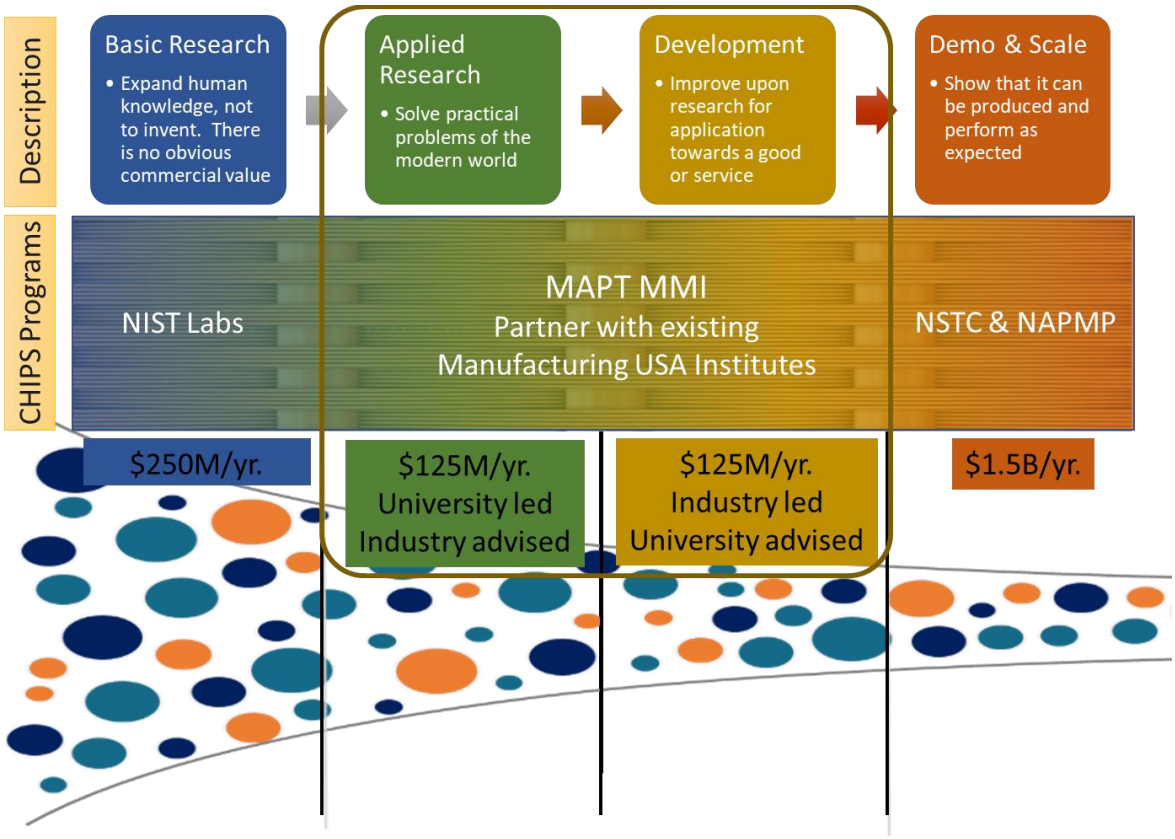



***Figure 11.*** *Microelectronics and Advanced Packaging Technology (MAPT) as a topic for a Microelectronics Manufacturing USA Institute (MMI) to bridge the Lab-to-Fab gap vision*

Furthermore, the institute needs a multi-dimensional plan which includes a robust supply of technologies and ideas that can align with, and feed into, the NSTC and the NAPMP **(Figure 11)**. This comprehensive plan from Basic Research through Demo & Scale as outlined above must include several factors and infrastructure for:

- Technologies that mature across the Technology Readiness Level (TRL) scale. This includes moving from Basic Research to Applied Research to Development and into Demo and Scale by designing and connecting all parts of the CHIPS Act along with existing innovation infrastructure.
- Technologies across the full stack, spanning from materials and devices through to the packaging and end-application, via interlocking multidisciplinary research.
- The full supply chain from materials through packaged and tested chips
- R&D on different time horizons of 3-5 years, 5-10 years, 10-15 years

This is a complex system with different requirements for different layers, nodes, and end markets.

Although there are many reasons to do this, the biggest needs for a super-sized institute combining Microelectronics and Advanced Packaging Technology are as follows:

1) Microelectronics and Advanced packaging Technology (MAPT) R&Ds need to be co-developed to maximize performance, minimize cost, and meet the stringent requirements of future technology systems such as autonomous vehicles, energy-efficient AI, and high-performance data centers. Splitting them would lead to optimization of one at the performance cost of the other. Performance potential can only be achieved by keeping them together throughout the R&D phases and codeveloping technical solutions. The future of microelectronics will be integrating heterogeneous technologies in three dimensions which required close co-design and optimization throughout the applied research and the development processes.
2) Industry must collaborate to gain and maintain competitiveness. Splitting microelectronics and APT would lead to bifurcation of the industry partners because industry does not have the resources (membership dues and manpower) or risk-tolerance to join multiple institutes.
    a) Industry is getting co-investment fatigue with the many options of joining NSTC, NAPMP, USA Institutes, DOD Commons, etc.
    b) Industry must collaborate with each other to be more effective. If industry is split into different institutes, there will be no collective learnings and direction setting.
3) Universities need to collaborate with each other across topics and disciplines to maximize effectiveness. R&D is a team sport and more effective when working together, as evidenced by the DARPA/SRC's JUMP (Joint University Microelectronics Program) program consisting of 6 university centers, having many universities supporting each research center and their corresponding six breakthrough challenges.
    a) For example, DARPA's ARPANET program in 1969, which became the foundation of the modern internet, was formed through a collaboration with UCLA, UCSB, University of Utah, and SRI

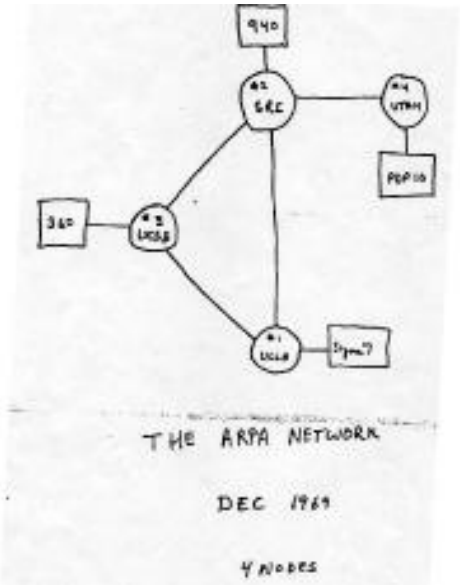



*Figure 12.*
*An early 'napkin' drawing of the concept for an ARPANET, courtesy of DARPA*

## C) Advantages of a second, smaller Institute

A second institute of 'standard size' that performs R&D on the topics of Virtualization, Visualization, and Automation (VVA) would be highly valuable to supporting US manufacturing. Automation of MAPT manufacturing would help solve two problems and would be imperative in achieving the goals outlined in the CHIPS legislation.

1. Automation could reduce the asymmetric advantage of manufacturing in lower-cost labor markets such as SE Asia. SE Asia has become a manufacturing hub for packaging because of the high manual labor needed for manufacturing coupled with the low cost of labor in the region. Lowering the labor intensity of packaging manufacturing could 'level the playing field' and make US manufacturing of packaging more competitive.
2. Automation of MAPT manufacturing could ease the semiconductor industry labor shortage by automating steps that are currently done manually, or that do not yet exist, and could be adopted with automation at its onset. Replacing these steps would lead to fewer employees needed per manufacturing site and thus minimize the labor shortage.

The VVA institute would have some strategic overlap with the MAPT institute on the edges of what is included for each, but they must work synchronously on technology development, technology transfer to manufacturing, and on EWD. Specifically, technology developed in one institute could add technology from the other and then transfer to a set of companies to achieve even greater impact.

## D) Partnerships

Partnering with others is critical and was discussed extensively in the response to Question 6.

Specifically, the Super-Sized MAPT Institute must be designed from the beginning to partner with the creators/operators of the NSTC, NAPMP, DOD Commons, DOE R&D, and NSF programs. Ideas for collaboration include, but are not limited to:

- Ability to co-fund collaborative research projects
- MMI use of facilities and infrastructure created by NSTC, MAPMT, DOD Commons.
    - Note it is our understanding that, due to NSTC, MAPMT, DOD Commons potentially having budgets ~5X larger than a $250M/year manufacturing institute recommended in this paper, these adjacent programs should have a heavy emphasis on building innovation pipeline infrastructure including tools, equipment, and facilities that does not currently exist. MMI R&D projects, along with other programs' R&D projects, would be users of that infrastructure and should be fully integrated with those programs.

- Leadership of each of the NSCT, NAPMP, and MMI should participate in a Leadership Council which helps direct and coordinate the activities of each to make them cohesive.

Q8. What membership and participation structure for a Manufacturing USA semiconductor institute would be most effective for ensuring participation by industry, academia, and other critical stakeholders, particularly with respect to financial and intellectual property obligations, access, and licensing? Based on your knowledge of current Manufacturing USA institute practices, are the needs of potential semiconductor institutes different than for other institutes?

*[Note: In addition to the response below, please reference the response to Question 6]*

We support the current general Manufacturing USA tiered membership model with project and access rights based on membership level. However, we suggest additional 'blue stamp' access for Diversity, Equity, and Inclusion (DEI) organizations, and small businesses. We also suggest a means to ensure a longer-term commitment from 'gold' (highest)-tiered membership, for an additional 5 years for joint R&D projects. This commitment should include a requisite DEI for Education and Workforce Development (EWD) component.

Government should not fund specific R&D, workforce development and other programs in perpetuity, but rather should use seed funding that creates and builds an institute that can operate in perpetuity with industry as the primary funding source. Only if industry is the primary funding source will it be industry-aligned and industry-serving. An estimate is that government would continue to get value form the institute and would therefore desire to fund it. Looking at other similar models, 20- 30% of revenue for effective existing collaborations comes from government. IP rights, governance, revenue models, and operations should be structured similarly to other institutes and incorporate best practices that can be borrowed from them. A few key points:

- Must be industry-led, have government oversight, and strong academic partners and be highly inclusive of the broad ecosystem
    - Inter-academic collaboration is important because of the high degree of technology required for success in the industry
- IP rights have to be balanced to allow industry members to profit from them while also recognizing the value creation by academia.
    - IP models' balance must include different options, perhaps some IP will be made publicly available while other IP will offer a high-competitive advantage for

sponsoring member(s) and therefore should provide some terms of exclusivity or protection.

- Manufacturing continues to add more advanced materials into the manufacturing process, including materials that can be reproduced but are not always well understood scientifically. Additionally, new materials need to be assessed for environmental health and safety which needs to be part of the research process.

The membership structure should be adaptable and flexible to encourage participation from all parts of the ecosystem, including industry (large and small business), defense, academia, government, trade organizations, and non-traditional participants. There should be a low barrier to entry for participation in the institute and should include meaningful incentives to attract members of special interests such as underrepresented minorities, woman, and veterans.

Membership should require a multi-year commitment but will have flexibility to allow members to shift from one type of membership to another. This will ensure that their membership category is aligned with their organization's needs and that they are maximizing the benefit from their organization.

Membership will be done on a Tiered basis with different costs and different rights/benefits:

| Tier | Description |
|---|---|
| Tier 1 | Large companies: manufacturing, fabless, equipment, materials, EDA, leading |
| Tier 2 | Mid-size companies, defense, participating academics |
| Tier 3 | Small companies, government labs, incubators, following academics, trade |

International members aligned with US interests will not only be permitted but will be encouraged to join and participate. For example, TSMC, Samsung, NXP, TEL, and many others are leaders in the semiconductor field with facilities in the US. It is important to attract organizations like this to have a more complete membership profile with potential to perform even more manufacturing in the US. These will comply with existing and future regulatory requirements.

## Section 3: Strategies for Driving Co-Investment and Engagement

Q9. The authorizing statute for Manufacturing USA requires at least an equal non-federal co-investment in Manufacturing USA institutes to match the federal investment. From your perspective, what are the most significant considerations to garner support for the required co-investment for a Manufacturing USA semiconductor institute? What is the anticipated impact of the new Investment Tax Credit (ITC) for industry established in the CHIPS Act on the level of investment in the new Manufacturing USA semiconductor institute(s), in facilities, including for manufacturing equipment and construction? How might a Manufacturing USA semiconductor institute be set up to best leverage the Investment Tax Credit?

The semiconductor industry needs to be at the forefront of cutting-edge development and ideas, but economic pressures do not always allow them to invest in such endeavors. These hurdles are especially great for small business. A shared mission and goal with academia and government will help alleviate some of that burden while pushing technology forward for the good of the country. Government subsidies for research also allows industry to push into a higher risk tolerance that they cannot otherwise afford. Correspondingly, industry must see a direct path for returns of investments in an endeavor such as a Manufacturing USA Institute.

To maintain financial support from industry, the Institute's technical direction must be industry led with advisory support from academia and government. To attract and continue support for the required co-investment, industry must realize value from financially supporting the Institute. For that to happen, the work of the Institute must have three important qualities:

1) Relevance - The Manufacturing USA Institute must be relevant to the industry's needs by aligning with their current and future objectives. Corporations are under great economic pressure, so to invest in an institute, they need to justify the cost with the future potential value-add to their business. Industry, however, is not the only source of cost share. State, local, and regional governments should provide important, indirect cost share through regional support and public awareness. Similarly, their indirect contributions must be relevant to the objectives of economic development.
2) High Quality - A Manufacturing USA Institute must be able to provide its members with the best researchers, facilities, and employees for the workforce. Rather than relying only on researchers in the top 5 research institutions, the Institute would ensure quality through diversity. By engaging future talent across a diverse community, the result will be more innovation, opinions, solutions, and ideas. The Institute needs to provide the venue to

bring together all aspiring best researchers to be mentored by the industry's seasoned professionals.

3) High Volume – With diversity in members comes diversity in interests. Therefore, the Institute must have a high enough volume of research covering a large breadth of topics to ensure all members see a critical mass and sufficient value to address their ever-evolving business needs.

These three factors can be achieved with tight integration between university, industry, and government to further ensure industry continues to financially support the institute. This alignment must be done at a scale relevant to industry and should ideally resemble SRC's Industry Liaison program. The Liaison Program is a powerful partnership that brings together university researchers, graduate students, and industry R&D experts to create profound impact. The Program's goals are:

- Develop Tomorrow's Workforce - Create a positive experience for student researchers that leads to a career in the semiconductor/microelectronics-related field and helps to growth the semiconductor workforce talent pipeline in a diverse and inclusive way
- Align Research Relevance - Maximize the research relevance to projected industry needs
- Transfer Technology - Minimize the time required for the research results to make an impact on the semiconductor industry, and identify potential patents and insights that may benefit member companies

A second mechanism for achieving the three qualities list above is for the institute to create large academic research centers that provide maximum value to industry, academia, and government. Research centers such as Texas Analog Center of Excellence (TxACE)[18] are excellent examples of collaborative efforts among these three vectors.

The new Advanced Manufacturing Investment Credit enacted as part of the CHIPS and Science Act of 2022 ("CHIPS Act") is a vital complement to the semiconductor grant program also enacted as part of the CHIPS Act. These important federal incentives indirectly support additional funds for important semiconductor research and innovation that aligns well with the mission of the Institute.

[18] https://txace.utdallas.edu/

Q10. For the required non-federal co-investment for a Manufacturing USA semiconductor institute, with respect to the different types of co-investments (e.g., cash, equipment donations, facilities access, etc.), are there factors unique to the semiconductor industry that would impact how the co-investment could be structured to best support the institute?

There are several factors that make the semiconductor industry unique as described in the response to Question 6. Two of these factors should be considered for how the co-investment could be structured.

The first factor is the high R&D intensity (R&D investment/revenue) of the industry, second only to the pharmaceutical industry **(Figure 13)**. On average, 20% of a company's revenue is spent on R&D costs[19]. Because of this, the institute should allow co-investment contributions from industry to be in the form of internal R&D activities that support specific projects competitively selected by the institute to be performed by the company offering the co-investment. That is, if Company A is selected as a performer on a $2M R&D project, some portion of the co-investment of that project could include work performed and paid for by Company A.

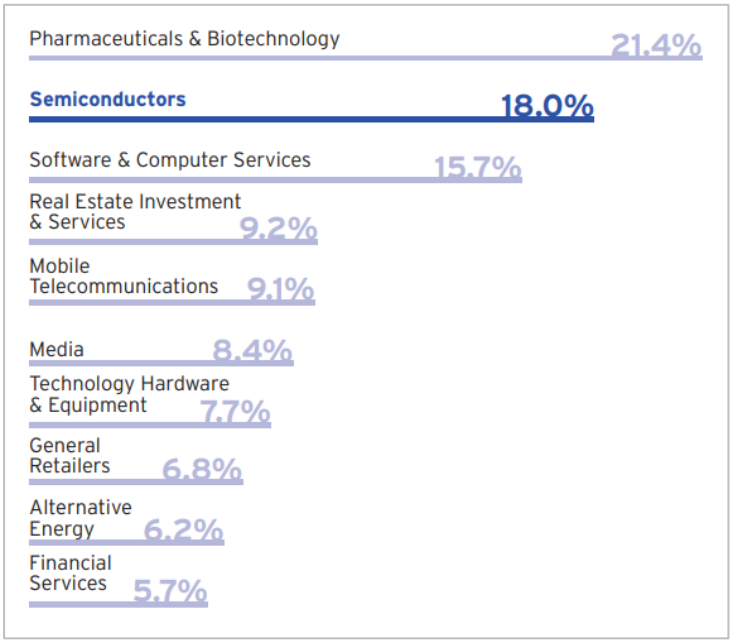



***Figure 13.*** *R&D expenditures as a percentage of sales by industry*

The second unique quality to the semiconductor industry is the high capital expenditure requirements to build and operate manufacturing fabrication, or 'fab' facilities. A compounding issue to the high capex for fabs is the decoupling in the industry between foundries that manufacture, and design companies that own a small amount of equipment which requires them to outsource manufacturing tasks. As part of co-investment contributions, foundries will be able to provide access to a variety of fab manufacturing facilities. Design companies will contribute co-investment software, IP blocks, and design expertise to help R&D performers create better technology.

[19] www.semiconductors.org/wp-content/uploads/2022/11/SIA_State-of-Industry-Report_2022.pdf

**Q11.** What arrangements for co-investment proportions and types could help a Manufacturing USA semiconductor institute sustain operations in the absence of continued federal support?

The institute must be formed to align with industry's needs to be successful, and in doing so, industry, academia, and non-federal government will provide financial support as co-investment. Co-investment from the semiconductor industry for collaboratively funded R&D is already happening with leading companies in the industry currently contributing millions of dollars, independent of federal support, to collaborative R&D in such programs as those administrated by SRC. This model establishes that co-investment of R&D by industry can sustain operations in the absence of continued federal support.

The success of this model can be attributed to the fact that the collaborative R&D creates value for industry members and is aligned with industry needs. However, existing models for collaborative R&D in semiconductors is limited in size and scope by the R&D funds that industry can allocate to technology at this readiness and risk level. Typically, less than 10% of proposals submitted have sufficient collaborative industry funding to be selected for funding. With federal support, the collaborative R&D work needed to meet the NIST, and Manufacturing USA objectives listed in the RFI announcement could be met.

Co-investments for the institute will come in the form of cash from membership dues and from 'fee for services' while in-kind contributions will be made by universities, industry members, national labs, and others. A MAPT institute which includes the scope of microelectronics and advanced packaging technology together for a $250M/year budget could achieve cost-matching of 1:1 at startup with the opportunity to growth throughout 5-year federally supported period.

**Q12.** A Manufacturing USA semiconductor institute should support domestic competitiveness. How should relationships with foreign entities be structured or constrained to support domestic manufacturing priorities while maximizing the opportunities to leverage international expertise and resources? In what circumstances should the Manufacturing USA Semiconductor institutes and NIST as the federal sponsor, consider membership requests from foreign-owned businesses?

As the semiconductor industry fractured into manufacturing specialties such as Chemicals & Materials, Design, Fabrication, Packaging and Test, geographic regions emerged as hubs of the supply chain. This regional specialization has enabled global economic growth for over 40 years and the continuation of Moore's Law well beyond what a single actor, alliance, or region could accomplish alone. Although this regional growth enabled global economic prosperity, it has

resulted in a growing economic interdependence across regions, and therefore, supply chain fragility and national security risks.

To minimize this risk, the US needs to partner with foreign companies that manufacture in the US as well as companies that provide services that support US manufacturing. Accordingly, these types of companies should be welcomed and encouraged to participate in the Manufacturing USA Institute as they are important contributors to NIST's objectives. Examples of foreign companies that employ many domestic industry personnel and support US manufacturing include: NXP, Samsung, TEL, SK Hynix, MediaTek, TSMC, ASM, Siemens, and ARM. The institute should welcome and encourage participation from these and other companies.

The criteria for allowing foreign companies to participate in the institute should be that they:

1) Support US manufacturing while having some presence in the US
2) Do not have headquarters or majority ownership in nations of concern (China, Iran, Russia, North Korea, etc.)
3) Comply with existing and future international trade laws including ITAR, EAR, etc. Publications by The Department of Commerce's Bureau of Industry and Security should be used as a guide for determining admittance of companies with foreign headquarters.

Q13. How should a new Manufacturing USA semiconductor institute engage other existing Manufacturing USA institutes (https://www.manufacturingusa.com/institutes), including those awarded funds for work related to semiconductor manufacturing, and other manufacturing related programs and networks such as the Manufacturing Extension Partnership (https://www.nist.gov/mep) and the U.S. Department of Energy's Next Generation Power Electronics National Manufacturing Innovation Institute ("Power America")?

There are several ways for a new Institute to engage other existing Manufacturing USA Institutes. A great starting place would be for the Institute to share both operational and intellectual property models. Sharing best practices with other Institutes could be key to quickly and successfully launching and then operating the Institute before and after government funding. Leveraging knowledge among Institutes is a very low cost and high benefit activity.

Institutes should also share facilities and resources where applicable. The semiconductor industry has advanced manufacturing capabilities that could be made available to other Institutes. We also recommend that some of the new dollars that go to existing manufacturing institutes be dedicated to collaborative R&D projects between the MAPT MMUSAI and other institutes.

Joint R&D and workforce development projects should be approached together. This new Institute would share common interests with Power America, AIM Photonics, NextFlex, CESMII, and possibly other existing Institutes. By pooling funds from different Institutes, additional leverage can be obtained to make R&D dollars even more impactful. Additionally, bringing together Institutes that have similar interests, but different viewpoints and motivators, would result in more robust innovation.

### Q14. How should a Manufacturing USA semiconductor institute interact with State and local economic development entities?

The Institute should leverage resources from across the United States, which will also help regional development throughout the country, especially in regions that do not currently participate in or support semiconductor manufacturing. The central region of the US has excellent resources and talent that could contribute to the mission of the Institute if a working relationship could be developed with State and local economic entities. These states have many universities, national labs, and research professionals that could further contribute to both the industry and the Institute's mission. State and local economic entities could assist in furthering workforce development efforts to the benefit of all. An example of this is the state investments with IEDC (Indiana Commerce) in recent years, and the corresponding growth in Indiana with TSMC, Skywater, and MediaTek.

In the past few years, various companies have set up new fabs across the US. Intel announced a new $20 billion factory outside Columbus, Ohio that will also create 7,000 construction jobs and another 3,000 permanent jobs. Samsung set up a $17 billion factory in Texas. Also in Texas, Texas Instruments invested up to $30 billion in a new chips foundry, and Global Foundries set up a new chips factory in New York state. Wolfspeed-Cree spent $1 billion to expand a current plant in North Carolina, SK Group invested in a new U.S. R&D center, and Micron is expanding US production in NY and Idaho. However, each region has its own DEI challenges. A supersize Institute will be able to work with each regional area to develop an equitable workforce plan.

### Q15. How should a Manufacturing USA semiconductor institute coordinate with and inform standards development bodies on the need to modify existing or develop new standards as a result of this initiative?

As technology advances, it is inevitable that current standards will need to change, and new standards will need to be developed. The Institute will be made up of the best minds from

academia, industry, and government. Close communication should be kept with industry organizations, such as IEEE, SEMI, UCIe, and SIA to ensure the Institute's viewpoints and voice are heard. Quarterly check-ins between leaders of each organization would keep all parties working towards the same goals. Joint workshops or conferences are another tool to discuss and flesh out possible modifications to existing standards or development of new standards. The development of new and future standards should be included in Roadmap activities as well.

For education and workforce development, standard curriculum and certification programs could be developed for Operator and Technician level employees which could be developed by Community College and other two-year education programs as part of the institute. These programs would provide credentials to students and allow them to join manufacturing companies with the skills and credentials needed to begin working and contributing immediately.

# Section 4: Education and Workforce Development

**Q16.** How could a Manufacturing USA semiconductor institute best support advanced manufacturing workforce development and/or awareness at all educational levels (e.g., for K-through post-graduate students)?

As the semiconductor industry continues to grow, the US needs a workforce to support manufacturing infrastructure, build and maintain the facilities, and operate the factories producing the critical supply of semiconductors. There is currently an insufficient supply of trained and educated employees with necessary qualifications, and the future workforce needs are going to restrict progress towards the efforts outlined in the CHIPS Act. As companies progress on new manufacturing projects spurred by the CHIPS incentives, the industry will create over 235,000 construction jobs in the six-year build-out phase. Ongoing operational needs will generate 525,080 jobs, many of which will be in manufacturing, but also include workforce at all levels in the manufacturing supply chain[20].

In the research and design stages of the manufacturing process, the industry requires the best and brightest scientists and engineers with advanced degrees in multiple fields of relevance to the industry[21]. These fields include electrical and computer engineering, mechanical engineering, materials science and engineering, chemical engineering, industrial engineering, physics, chemistry, and mathematics, with additional skills in data science, automation and smart manufacturing, sustainability, machine learning, and artificial intelligence. Engineers with such educational backgrounds remain in short supply in the domestic semiconductor workforce as the semiconductor industry competes with powerhouse software companies that have more consumer-facing and recognizable brands. Job-hunting engineers are more familiar with these big brands and since they offer exceptional salaries young professionals often launch their careers there.

Engineers without such educational backgrounds cannot acquire it through on-the-job training or by short courses in a vocational setting. These skills can only be acquired from a multi-year, structured academic program with strong fundamentals in math, chemistry, and physics and a deliberate focus on the knowledge, skills, and abilities needed for jobs in the microelectronics and advanced packaging manufacturing industries. Access to enough of these highly educated engineers is critical to the development of our future generation of products and technology and to our ability to maintain the US semiconductor industry as the global leader.[22]

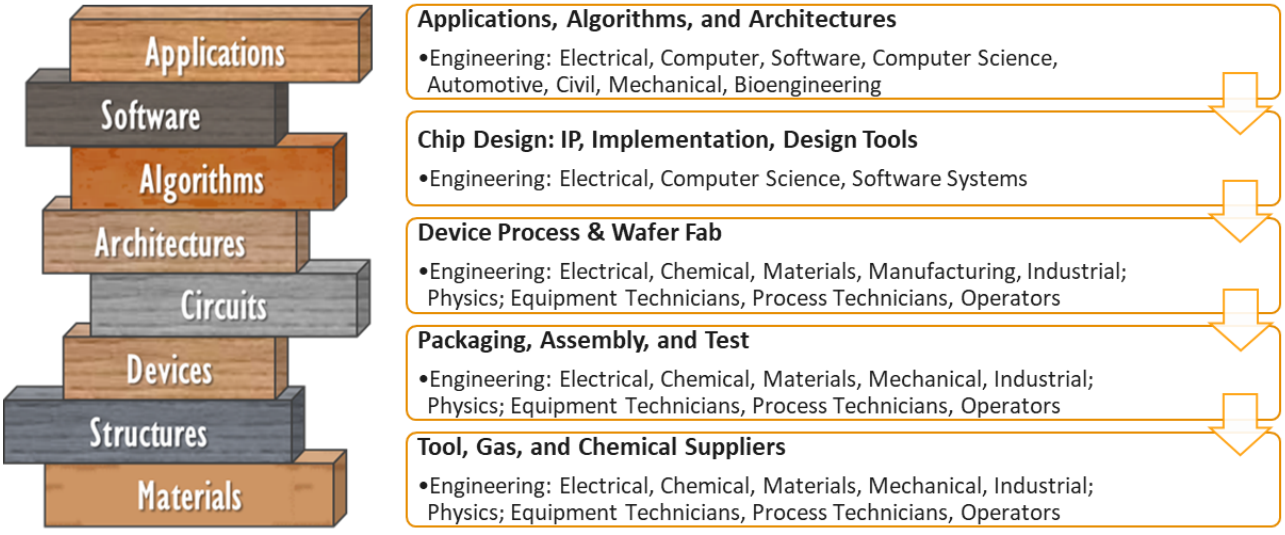
[20,21] www.semiconductors.org/wp-content/uploads/2022/03/Commerce-CHIPS-Act-RFI_SIA-Response_Final-1.pdf

[22] SIA, NIST Workforce RFI, https://www.semiconductors.org/wp-content/uploads/2018/11/NIST-workforce-RFI-august-2018.pdf (p. 5)

In the Fall of 2021, Purdue University hosted a workshop that assessed the skill requirements for both Microelectronics and Advanced Packaging workforce development[23]. The workshop provided a useful assessment of the needs and some suggestions for additional measures to build the semiconductor workforce. These included but are not limited to:

1) The need to attract more students to microelectronics and create degree programs and certificates across the entire supply chain.
2) The need for amplification of partnership models across academia, community colleges, industry, and government to articulate the knowledge, skills, and abilities of this new workforce, with special attention paid to hands-on training and online programs.
3) The need to scale investments to rapidly educate thousands of students which will require significant funding from and involvement by the federal government, industry, and schools that may not traditionally be strong in microelectronics or advanced packaging. This will require new models for collaboration and support across and between these organizations.

To address this "full stack" of technology and education needed for US semiconductor leadership, we should recognize the different skills needed in each area:




[23] https://engineering.purdue.edu/Engr/AboutUs/News/Events/purdue-microelectronics-and-advanced-packaging-workforce-development-workshop

Another emerging opportunity is to expand the education of students in the field of advanced packaging technology. The fundamental challenges are:

1) Disseminating US academic thought leadership in advanced packaging and heterogeneous integration beyond today's few leading faculty and institutions
2) Adding new facilities and new faculty across the US in advanced packaging and heterogeneous integration
3) Developing a culture where innovative ideas are supported by a new innovation pipeline and ecosystem with a path to commercialization

Packaging needs of the future will require very complex co-design and co-integration of diverse technologies as shown in Figure 14. Semiconductor education has traditionally focused on microelectronics, with an emphasis on devices, design, and systems. It has had little emphasis on packaging or its importance as an emerging area of innovation opportunity. Packaging requires multiple disciplines including electrical, mechanical, materials, chemical and industrial engineering, physics, chemistry, mathematics, as well as skills in data science, machine learning, artificial intelligence, sustainability, automation, and smart manufacturing. Collaborations across these disciplines is required for developing and implementing innovative, manufacturing-worthy packaging solutions. Education and workforce development must, therefore, be intentionally cross-disciplinary, with emphasis on critical thinking, problem solving, failure analysis, metrology and test, diagnostics, modeling (electrical, thermal, stress/mechanical, optical, materials), and sustainability.

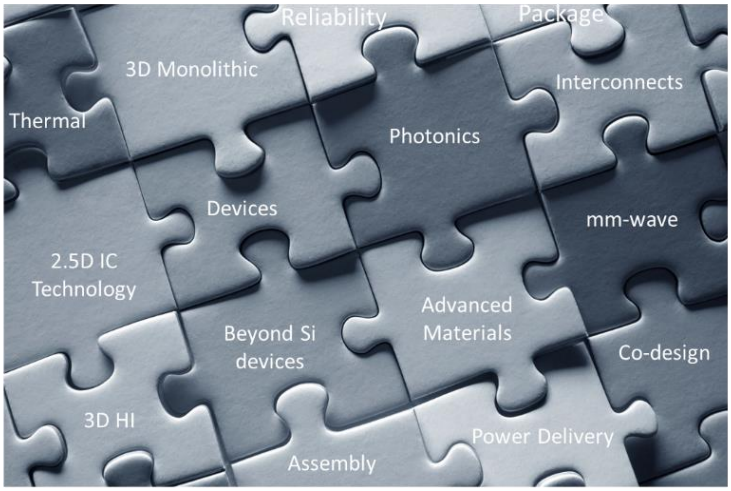



***Figure 14.*** *Illustration of the complex co-design and co-integration of technologies needed for advanced packaging technology*

Further, a critical barrier to advanced packaging education in academia is the lack of state-of-the-art packaging facilities, including wafer-wafer bonders, die-to-wafer bonders, advanced flip-chip bonders, substrate fabrication tools, plating stations, reflow ovens, packaging metrology tools, fiber-attach tools, and dielectric dispense and cure tools, among others. An obstacle for having access to these tools is cost; for example, a state-of-the-art flip-chip bonders with fine-alignment accuracy assembly can cost in excess of $1M; advanced wafer-bonders cost multi-million dollars. Such tools are also very complex to operate and maintain and require skilled and dedicated technical staff. Further, some of these tools require significant fab floorspace, making them expensive for cleanroom real-estate. A Manufacturing USA Institute should invest in academic infrastructure.

In summary, a Manufacturing USA Institute must be devoted to:

1) Partnering with undergraduate and graduate programs at research-intensive institutions that include emphasis on microelectronics and advanced packaging, providing both a strong disciplinary background and interdisciplinary, holistic understanding to complex problems
2) Partnering with undergraduate and graduate programs to expand the number of women and underrepresented communities in semiconductors, particularly working with Minority Serving Institutions
3) Training for technicians utilizing, among other institutions, two-year or community colleges

Q17. How could a Manufacturing USA semiconductor institute best engage and leverage the diversity of educational and vocational training organizations (e.g., universities, community colleges, trade schools, etc.)?

Specific and actionable recommendations for building the workforce to support a reliable semiconductor supply chain by leveraging the diversity of our secondary and post-secondary educational systems include:

1) ***Community Colleges****:* Train the workforce through the vast resources in Community Colleges, which are often the hidden crown jewels of the US economy. These should serve not just to train high school graduates, but also to expand the training and skills of employees currently working in the semiconductor industry and in manufacturing. Furthermore, these community colleges can help retrain and reskill employees from adjacent receding industries to prepare them for viable jobs in the semiconductor industry.

This system can also be used for military veterans who are re-entering the private workforce.

2) ***Scaling with hybrid virtual learning:*** Hybrid virtual learning could be used to educate and train many people simultaneously. For example, instead of 200 professors at 200 universities/colleges teaching 200 versions of the same topic to 20 students each, have one "best" professor provide virtual/MOOC (massive open online courses) lectures to 10,000 students at many colleges and universities.

3) ***Undergraduates:*** Attract and educate BS-level students to build, operate, and maintain the facilities, equipment, processes, and research needed for a semiconductor infrastructure.

4) ***Graduate Students:*** Build the research staff by further funding MS and PhD graduate students in academia and educating them on relevant topics in the field. This is important for creating more researchers and for creating more professors to mentor future researchers.

### Q18. How could a Manufacturing USA semiconductor institute best ensure that advanced manufacturing workforce development activities address the industry's priorities?

Because of the institute's partial governance and direction-setting by industry, institute WFD activities would systematically align directly with industry's priorities. While government-led programs have been effective for recruiting and retraining some portion of the general population, there is another portion of the population that does not generally consider government programs when looking for jobs or upskilling/reskilling to find new jobs. As such, creating a more comprehensive solution should include programs that are run and managed by industry and non-profit organizations through a Manufacturing USA institute program.

Industry needs will inform the institute's activities and priorities in the following ways:

- How new programs will prepare the workforce for industry's needs in 2-6 years
- How community colleges develop and implement technical curriculum with hands-on training, then partner with local businesses for on-the-job training as part of the industry-specific curriculum

- How to develop internships for students at all education levels so they can gain experience and a better understanding of what semiconductor manufacturing jobs entail
- Provide industry professionals who rotate into community colleges and universities to teach specific classes and courses. This first-hand account of industry will not only align students with manufacturing industry needs, but also inspire students to consider this career path.

### Q19. How could a Manufacturing USA semiconductor institute best leverage and complement existing education and workforce development programs?

The Manufacturing USA semiconductor institute would need to research and assess all current workforce development programs currently being run by other institutes. Additional research could be conducted in key industry cluster states and regions to identify current best practices and the strongest, most successful programs. The institute could identify gaps where programs need to be built, and opportunities for enhancement and support where programs are working well. Successful programs could be scaled and replicated in other regions, leveraging workforce development systems and infrastructure already in place. The institute could also advocate for the sharing of curriculum, training facilities, and clean rooms where possible.

In many cases, the Institute does not need to reinvent effective WFD programs but can minimize risk and expedite results by partnering with successful programs that already exist across the US. One example is the Scalable Asymmetric Lifecycle Engagement (SCALE) program at Purdue[24]. This program is focused on WFD for the defense sector and managed by NSWC Crane to train highly skilled US microelectronics engineers, hardware designers, and manufacturing experts. This program has over 200 students enrolled, 17 participating universities, and $30M of DOD funding.

A second existing program to consider partnering with is the National Nanotechnology Initiative's Education resources which spans "pre-K through gray"[25]. This program, in partnership with a MMI, could further expand and leverage the effort to get more students prepared for a domestic semiconductor manufacturing career.

SEMI, the global industry trade organization for the electronics manufacturing, also has extensive workforce development partnerships that should be included and leveraged for any EWD MMI programs[26].

[24] https://research.purdue.edu/scale/
[25] https://www.nano.gov/education-training
[26] https://www.semi.org/en/workforce-development/semi-foundation/partnerships

### Q20. What measures could assess Manufacturing USA semiconductor institute performance and impact on education and workforce development?

A key objective for the institute is to create the direct workforce needed to perform manufacturing, and the indirect support jobs required for a vibrant semiconductor manufacturing ecosystem. Creating a workforce that matches the needs of the industry and the broader ecosystem is required for successfully meeting the objectives. Further, creating jobs is an effective component for enhancing economic growth and strengthening national security. The key performance indicators needed to measure the institute's performance and impact on education and WFD would include:

- Number of students and workers trained, educated, and reskilled through the institute.
    - Track where institute graduates go for their initial employment following this training
- Magnitude of WFD programs
    - Number of Workforce Develop Programs which support Manufacturing Jobs including not just the operation of manufacturing equipment, but both direct and indirect jobs as described in the answer to Question 25.
    - Number of universities receiving funding (including geographic diversity)
- Student metrics
    - Number of graduating students entering the domestic semiconductor manufacturing workforce
    - Number of trained/sponsored students participating in domestic semiconductor manufacturing internships
    - Number of published papers co-authored with industry members and students
    - Number of underrepresented students participating in Institute-sponsored R&D projects.
- WFD program effectiveness
    - Develop and measure "student readiness" for industry careers through industry surveys to identify deficiencies and make improvements
    - Attendance of Institute created short-courses, tutorials, training, and educational webinars

### Q21. How might a Manufacturing USA semiconductor institute integrate research and development activities and education to best prepare the current and future workforce?

Research and development activities sponsored by the MMI will be an essential part of educating and preparing students for the workforce and creating new technology. The skills learned in performing research as a student will translate directly to their work in industry, academia, or government upon graduation. Through R&D activities, students will get hands-on experience of how to create the technology in a lab that will later be fabricated in manufacturing facilities. They will also get a better understanding of how nuanced the creation of technology can be. This R&D integration with students' education must be done at all levels of post-secondary education.

Several considerations should be made for the MMI to integrate, design, and align R&D with WFD needs relevant to industry in both the short and medium term. To make this actionable, the MMI should first collaborate with expert education and training organizations for developing industry-informed and pedagogically-sound education and training content. Technical resources (volunteers, tools, platforms etc.) for education and training must be included. Secondly, the MMI must specifying competencies and characteristics (knowledge, skills, behavior, and attitudes) for current and future roles in the semiconductor industry. And lastly, the MMI must increase outreach and awareness to potential students who will potentially become part of the semiconductor manufacturing industry in the future. This would require marketing initiatives to broad swaths of potential students that could be recruited.

To financially support this integration of R&D into EWD initiative the MMI should dedicate up to $50M per year over 5 years to support this work, perhaps 70% from government and 30% from industry. To ensure effectiveness, the MMI should develop complementary programs that align well with other government programs at NSF, DOD, Commerce, and elsewhere.

### Q22. How could a Manufacturing USA semiconductor institute help build a steady pipeline of skilled workers? What knowledge, skills and abilities will future workers need, and are there workers with those skills currently employed in other sectors?

To build a steady pipeline of skilled workers with the KSA's (knowledge, skills, and abilities) needed for the future of domestic semiconductor manufacturing, a holistic strategy must be employed. The simple idea of revising curriculum or funding more graduate students, while helpful, is too narrowly focused to meet all of the semiconductor communities' broad needs. To build the steady pipeline of students the MMI should following the following five steps:

1) **Quantify the needs:** First, we must perform a Needs Analysis to map and analyze the projected number of each type of employee needed. This analysis must include details of skillsets, training, education, and experience needed for industry, government, and academia for each of the next 10 years. This can be compared to projections of available, then the gaps can be determined and quantified.
2) **Minimize attrition:** Second, we must understand and quantify where attrition is happening, including losses to adjacent industries, losses to other countries, retirements, etc., then develop and implement plans to minimize these losses.
3) **Reskill adjacent workforces:** Third, we must identify and recruit from adjacent manufacturing industries to serve as a source of workers through either upskill or reskilling. Included here as an enormous resource are veterans leaving the military to rejoin the private sector.
4) **Grow the talent pipeline (students):** Fourth is to train and educate more students into the industry. It must begin with gaining the attention and interest of future innovators from all demographics across the US, so a well-designed outreach and recruitment strategy is needed. It will also be necessary to evaluate which existing programs are working effectively and scaling them, while also creating new programs for all post-secondary degrees, including AA, BS, MS, PhD.
5) **Diversity, Equity, and Inclusion:** Fifth, to augment the existing workforce and create a sufficient supply of workers for the new workforce, we must recruit more women and under-represented minorities into the semiconductor field. Engaging with these communities by co-hosting events at their sites or where they meet will be more effective than just inviting them to participate in the typical semiconductor events dominated by Caucasian and Asian males.

Q23. How could a Manufacturing USA semiconductor institute broaden the talent base (i.e., embrace diversity, equity, inclusion, and accessibility; reach women and minority communities, engage non-traditional workers, engage separating service members, veterans, and families) to modernize the workforce?

The need is clear. Women, underrepresented minorities, and veterans are a great resource that could be further participating in, and benefitting from, the domestic semiconductor manufacturing industry. Not only would their expanded participation benefit them through high paying, good quality, reliable jobs but the US would benefit by their participation as they help to strengthen the economy and national security.

There are many ways that the MMI could broaden the talent base by engaging with these communities. It is important that the engagement be designed to meet with these communities where they are. That is, more than just inviting these communities to join MMI activities, MMI activities should be planned and scheduled where these communities currently exist. Examples could be at Society of Women Engineering (swe.org) and the National Society of Black Engineers (nsbe.org) events. In fact, the MMI should sponsoring activities at each of these organizations' national conferences to help raise awareness within these communities about the opportunities in semiconductor manufacturing while also listening to these organizations about what is important to them and how the MMI could be shaped to make it appealing to their members. Further, the MMI could hold annual meetings, industry talks, and tutorials at these organizations' conferences and members' facilities.

Additional ways to broaden the talent base is to align with the Biden administration's Justice 40 initiative. With this initiative, "the Federal Government has made it a goal that 40 percent of the overall benefits of certain Federal investments flow to disadvantaged communities that are marginalized, underserved, and overburdened by pollution[27]." By working with these communities, the semiconductor manufacturing industry would recruit valuable new talent with broader ideas. The communities that would be identified for recruiting would be found on the interactive map available here, with a screenshot in Figure 15.

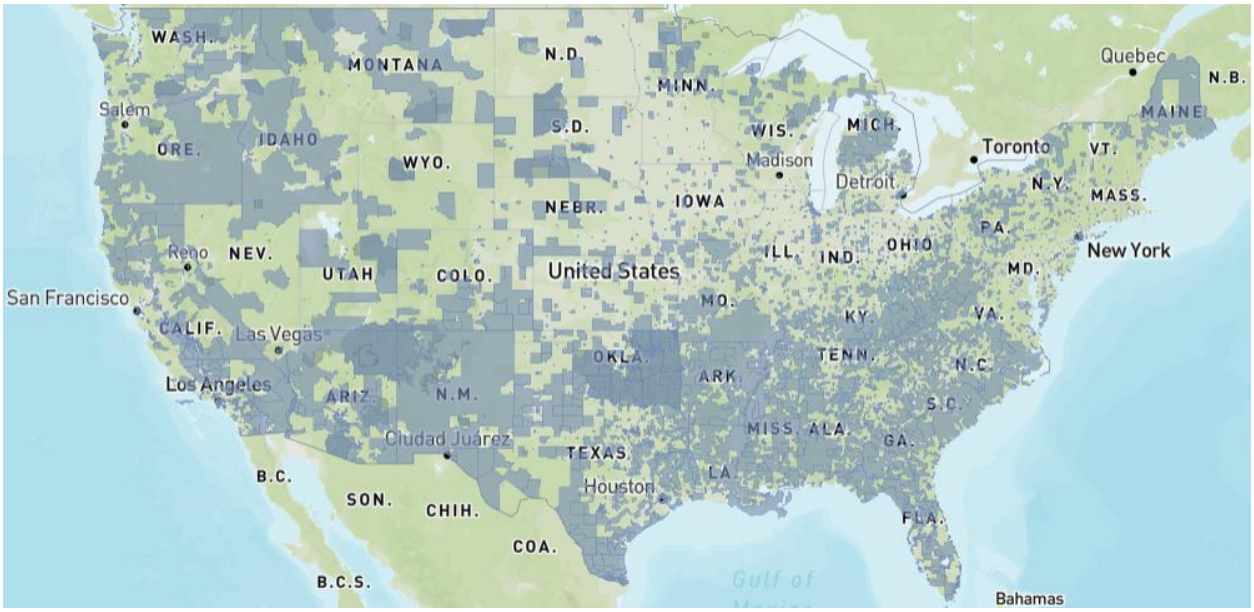



*Figure 15. Screenshot of interactive map identifying Justice 40 disadvantaged communities*

[27] www.whitehouse.gov/environmentaljustice/justice40/

Q24. What type of education and workforce development activities should a Manufacturing USA semiconductor institute support (e.g., curricula, online education, hybrid, entrepreneurship opportunities, credentialing, regional development, train the trainers, internships/ apprenticeship, learning labs, etc.) and why?

The new institute should start EWD activities with those that have demonstrated success in adjacent industries at existing institutes. Specifically, the new institute should use the methods employed by both the AIM Photonics Institute in photonics and the Power America institute in wide bandgap semiconductors. Both institutes have had success educating and developing the workforce needed for their respective industries.

The institute should develop and promote educational resources which could span from asynchronous through 1:1 industry mentoring. Asynchronous and live educational resources should be made broadly available to people that could potentially contribute to the institute's mission. These resources would include technical webinars, tutorials, and short courses. Industry mentoring would have a more limited audience but could be an effective method for high-potential students or employees with capacity for substantial growth in the field.

Beyond this, a super-size institute will need to implement larger-scope EWD programs that could only be accomplished with the resources available to a super-sized institute. This should include ways to work with industry, government, and academia.

Several other EDW activities were included in prior responses and are copied below for quick reference:

*From response to Q17*

- *Community Colleges:* Train the workforce through the vast resources in Community Colleges, which are often the hidden crown jewels of the US economy. These should serve not just to train high school graduates, but also to expand the training and skills of employees currently working in the semiconductor industry and in manufacturing. Furthermore, these community colleges can help retrain and reskill employees from receding industries to prepare them for viable jobs in the semiconductor industry. This system can also be used for military veterans who are re-entering the private workforce.

- *Scaling with hybrid virtual learning:* Hybrid virtual learning could be used to educate and train many people simultaneously. For example, instead of 200 professors at 200 universities/colleges teaching 200 versions of the same topic to 20 students each, have

one “best” professor provide virtual/MOOC (massive open online courses) lectures to 10,000 students at many colleges and universities.

*From response to Q18*

- Develop internships for students at all education levels so they can gain experience and a better understanding of what semiconductor manufacturing jobs entail.
- Have industry professionals rotate into community colleges and universities to teach specific classes and courses. This first-hand account of industry will not only align students with manufacturing industry needs, but also inspire students to consider this career path.

*From response to Q21*

- To financially support this integration of R&D into EWD initiative, the MMI should dedicate up to $50M per year over 5 years to support this work, perhaps 70% from government and 30% from industry. To ensure effectiveness, the MMI should develop complementary programs that align well with other government programs at NSF, DOD, Commerce, and elsewhere.

# Section 5: Metrics and Success

The MMI should have ambitious objectives that weave into the objectives and operational models of the associated R&D programs from the CHIPS Act, including the NSTC, NAPMP, DOD Commons, and NIST Labs research. The MMI should be designed to reduce supply chain risks, strengthen national security, and accelerate global leadership. Additionally, reducing the barriers to domestic manufacturing of semiconductors must be a main objective that is reflected in the metrics. This includes improving the cost-competitiveness of domestic manufacturing, and ensuring the availability of a talented, trained, and well-educated workforce. A critical part of this is to ensure that R&D programs enable not just technical leadership, but also the ability to manufacture those technologies domestically unlike the fate of other technologies now being manufactured in China. For example, the technology used for LED displays was developed in the US, but the manufacturing was ultimately scaled in China. We can do more to improve domestic manufacturing.

The Manufacturing USA semiconductor institute should be measured against the mission that Manufacturing USA clearly defined in the NIST webinars held in October shown below in Figure 16.


*Figure 16. Vision and Mission of Manufacturing USA institutes presented at the October webinars by NIST*

Further, a recent report[28] describing the impact of Manufacturing USA Institutes should be used as a guide for developing additional metrics aligned with existing and operating institutes. An example of metrics from that report that this institute should broadly support is shown in the following Table 1.

[28] https://www.manufacturingusa.com/reports/mfg-usa-report-congress-fiscal-year-2021

| Specific Metric | Unit of Measure | FY 2020 | FY 2021 |
|---|---|---|---|
| **Metric Category 1 – Impact to U.S. Innovation Ecosystem** | | | |
| Organizations with institute membership agreements | Total number of memberships | 2,013 | **2,320** |
| Diversity of member organizations | Number of large manufacturers (more than 500 employees) | 355 | **407** |
| | Number of small manufacturers (500 or fewer employees) | 895 | **1053** |
| | Number of academic members (universities, community colleges, etc.) | 459 | **516** |
| | Number of other entities (government members, government laboratories, not-for-profits, etc.) | 304 | **344** |
| **Metric Category 2 – Financial Leverage** | | | |
| Federal investment | Federal base funding in the fiscal year | $163 M | **$127 M** |
| Co-investment | Cost-share expended and federal funding not part of the base federal funding in fiscal year | $262 M | **$314 M** |
| Pandemic Response | Federal special pandemic projects funding | N/A | **$40 M** |
| Total Expenditure | Total institute expenditures in fiscal year | $425 M | **$481 M** |
| **Metric Category 3 – Technology Advancement** | | | |
| Active research and development projects | Number of ongoing projects | 534 | **708** |
| Key project objectives met | Percentage of key project milestones met | 79% | **82%** |

*Table 1. Example of collective Manufacturing USA Institute metrics that the MAPT Semiconductor Institute will contribute to*

We recommend that the metrics of the MMI be comprehensive, achievable, measurable, and transparent. This could be a scorecard which captures quantitative metrics aligned with NIST's and Industry's objectives. Table 2 below illustrates an example of a partial scorecard that could be used, with corresponding time-based metrics across five categories, to measure the institutes performance and ensure alignment.

***Table 2.*** *Example table of quantitative metrics*

| Metric | Year 1 Target | Years 2- 5 Target | Years 5+ Target |
|---|---|---|---|
| **Operations & Finance** | | | |
| Number of members | >50 | >100 | >125 |
| Overhead rate | <10% | <10% | <10% |
| Cost share | >1:1 | >2:1 | >4:1 |
| **Technical** | | | |
| Number of patents, papers, etc. | 0 | 500 | 5,000 |
| Number of US manufactured products | 0 | 20 | 200 |
| Number of tech transfers to NSTC, NAPMP & US manufacturing | 0 | 100 | 1,000 |
| **Education & Workforce Development** | | | |
| Number of students funded | 100 | 5,000 | 20,000 |
| Number of students hired as interns/FTEs into domestic manufacturing | 0 | 1,000 | 10,000 |
| Short-course, tutorial, training attendance | 100 | 1,000 | 10,000 |
| Training certifications earned | 0 | 200 | 2,000 |
| **DEI** | | | |
| % Women & underrepresented minorities educated & trained | 20% | 40% | 50% |
| % Women & underrepresented minorities as members | 20% | 40% | 50% |
| Number of US states represented | 20 | 35 | 50 |
| **Impact** | | | |
| Supply Chain: Dual sourcing of critical materials & equipment | N/A | 3 | 8 |
| US Manufacturing: Increase in US share of global manufacturing | N/A | 12 | 15 |
| National Security: Domestic demonstration of advanced technology | N/A | 3 | 30 |

Q25. What metrics could be used to best evaluate the performance of a Manufacturing USA semiconductor institute in accelerating innovation, and any associated impacts on economic competitiveness and national security? Are there sector-specific metrics for an institute in the semiconductor technology space?

Although the US is globally competitive in semiconductor design, the US lags globally in manufacturing portions of the supply chain as illustrated in **Figure 17**. This highlights that US manufacturing is dependent on foreign manufacturers for Equipment, Materials, Wafer Fabrication, and OSAT (outsources semiconductor assembly and test)[29].

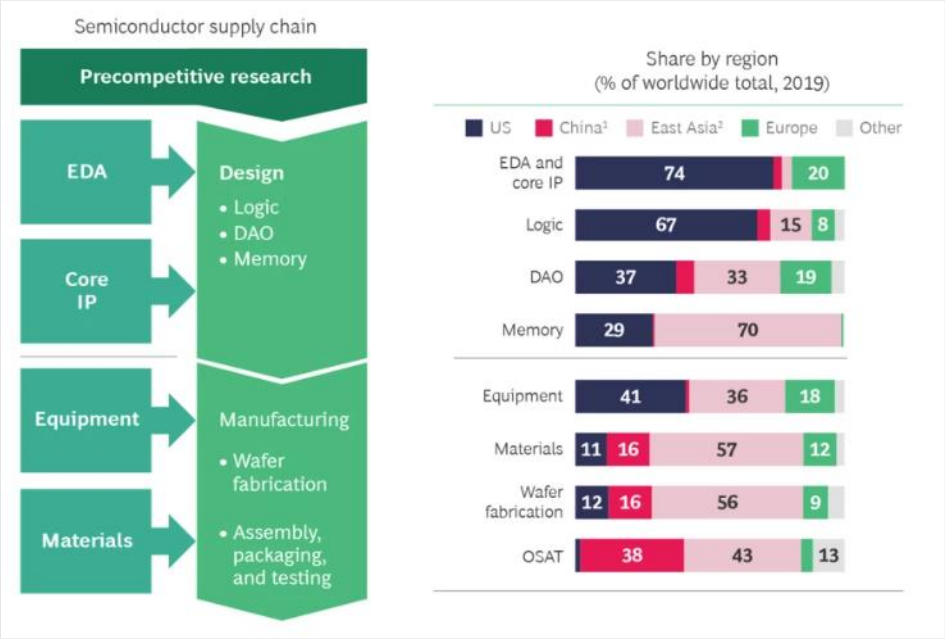



*Figure 17. Regional comparison of supply chain market share.*

To achieve the objectives defined by NIST, the MMI should have clear, quantitative, and semi-quantitative metrics to evaluate the performance of the institute operation, the quality and relevance of the R&D performed within the institute, and the impact that the institute provides. Although each of these categories is intertwined with the others, the following metrics can be considered elements of each category for accelerating Innovation, Economic Competitiveness, and National Security as illustrated in **Figure *18***.

[29] www.bcg.com/publications/2021/strengthening-the-global-semiconductor-supply-chain

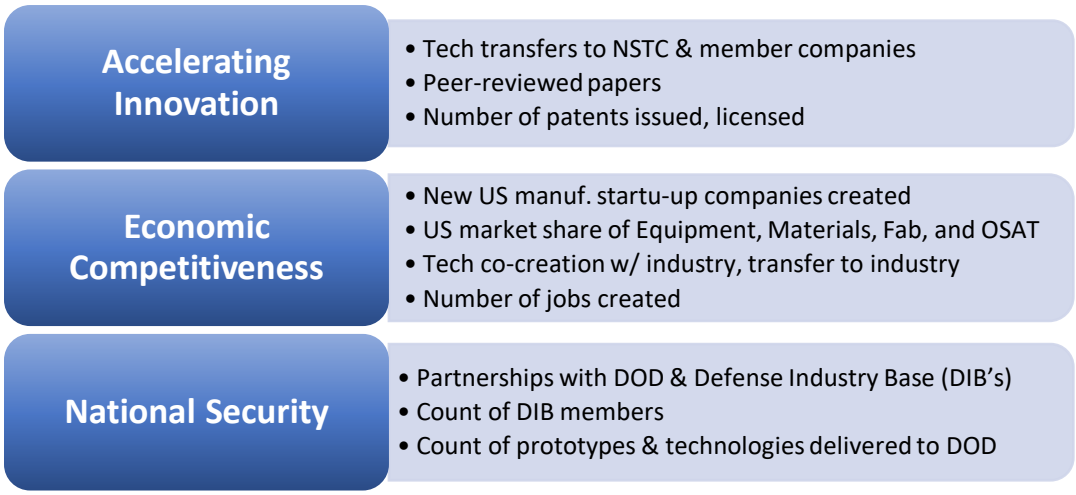



*Figure 18. Metrics to determine institute performance regarding innovation, economic competitiveness, and national security*

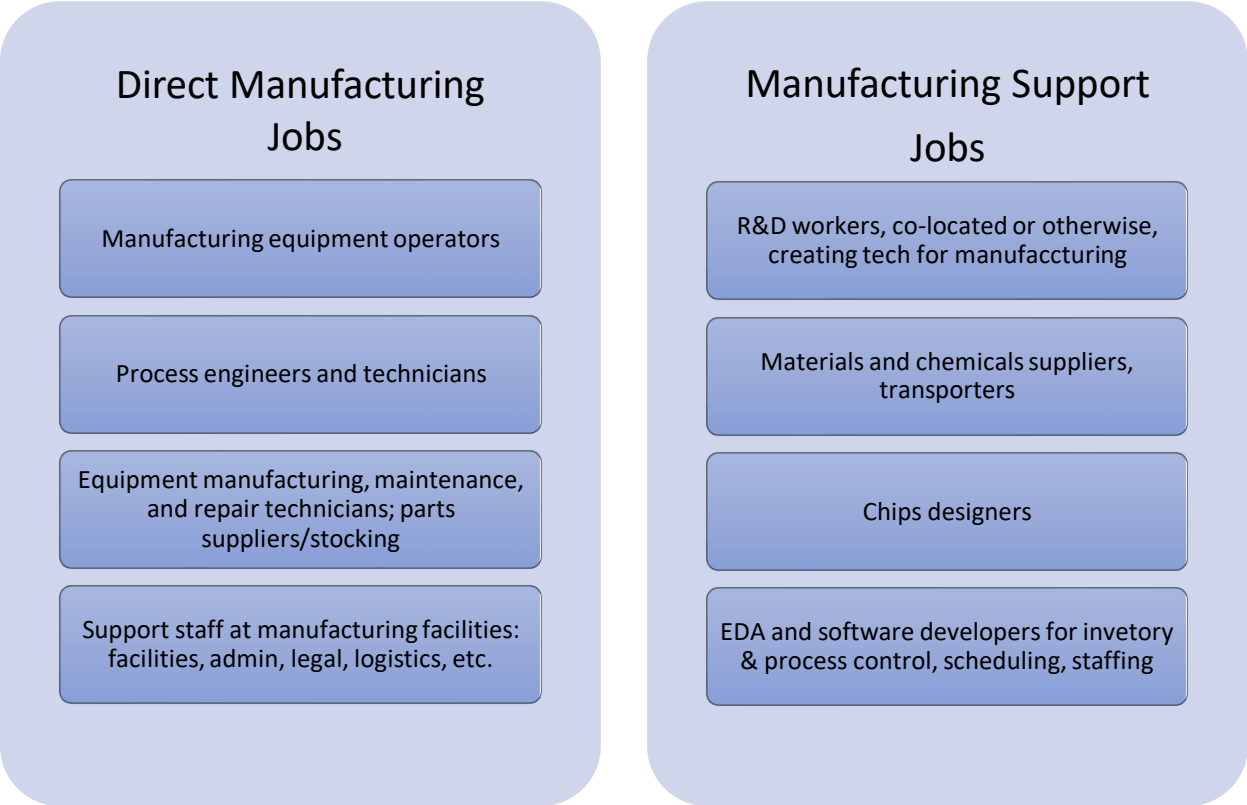
Table 3 provides specific examples of the materials and equipment that the domestic semiconductor supply chain is dependent on and draws an analogy to the onshoring of materials and equipment by the automotive industry. By following Auto's example, the domestic semiconductor manufacturing industry can increase competitiveness by having a more predictable and reliable supply chain by including more domestic suppliers.

| | Materials | Equipment |
|---|---|---|
| Auto | steel, rubber, plastics and aluminum, glass, chips, batteries | Robotics, Inspection, Test |
| Semiconductor | silicon wafers, metals, photoresist, solvents, precursors | Lithography, Processing, CVD, PVD, Electrodeposition, Plasma Etch, Thermal Processing, Grinding, Inspection, Test, Cleans, W2W/D2W Bonding |

*Table 3. Comparison of Materials and Equipment on shored for the Auto industry and corresponding needs for the semiconductor industry.*

When measuring progress in Economic Competitiveness resulting from Institute, it is important to include the number of jobs created. When measuring jobs created, we must determine an appropriate criteria for which to quantify jobs created. For the purpose of Economic Competitiveness, it is recommended that a broad approach - including manufacturing and manufacturing support jobs - be included, alongside factory workers assembling parts or operating equipment. We take this approach because it more accurately recognizes the domestic economic

contributions. Examples of jobs that should be created and counted towards Economic Competitiveness include:




Q26. What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute on education and workforce development in support of U.S. competitiveness?

*[Note: This question is similar to Question 20 above, and thus the response is similar.]*

A key objective for institute is to create the workforce needed to perform manufacturing, and the indirect support jobs required for a vibrant semiconductor manufacturing ecosystem. Creating a workforce that matches the needs of the industry and the broader ecosystem is required for successfully meeting the objectives. Further, creating jobs is an effective component for enhancing economic growth and strengthening national security. Aligned with that is setting goals associated with workforce development. These could be:

- Number of students and workers trained, educated, and reskilled.
    - Track where new MMI graduates go for their initial employment following this training

- Magnitude of WFD programs
    - Number of Workforce Develop Programs which support Manufacturing Jobs including not just the operation of manufacturing equipment but both direct and indirect jobs as described in the answer to Question 25.
    - Number of universities receiving funding (including geographic diversity)
- Student counts
    - Number of graduating students entering the domestic semiconductor manufacturing workforce
    - Number of trained/sponsored students participating in domestic semiconductor manufacturing internships
    - Number of published papers co-authored with industry members and students
    - Number of underrepresented students participating in Institute sponsored R&D projects
- WFD program effectiveness
    - Develop and measure "student readiness" for industry career through industry surveys to identify deficiencies and make improvements
    - Count number of attendance of Institute created short-courses, tutorials, training, and educational webinars

Q27. What type of metrics could be used to best evaluate the performance and impact of a Manufacturing USA semiconductor institute in establishing and expanding the U.S. semiconductor manufacturing ecosystem?

For measuring the impact of a Manufacturing USA Institute on the expansion of the manufacturing ecosystem, we can look at how the ecosystem is being brought together and the magnitude of the programs that will lead to manufacturing. Beyond the WFD metrics listed in the response to Question 26 above, for measuring the expansion of the ecosystem, the participation, diversity, and other characteristics of organizations supporting the institute can be evaluated. This would include not just the number but also the financial commitments, participation in institute events, and the member retention for subsequent years.

Additional metrics that are related more directly to domestic manufacturing could include number of technologies transferred from Institute R&D projects directly to industry labs and to other CHIPS Act programs such as NSTC and NAPMP. Metrics to consider as proxies in the earlier years of the Institute could be number of papers, patents, partnerships, and interactions. As the institute ages, we could make more direct measurements such as products with Institute IP that are

manufactured domestically. Measuring the increase in dual-sourced critical materials and equipment would also indicate an increasing domestic ecosystem.

We can also use growth of domestic manufacturing as an indirect measure of the success of the institute. To measure this domestic manufacturing growth, we can consider ***three categories***, which are: (1) expansion of domestic manufacturing capacity; (2) manufacturing employment expansion; and (3) expansion of supply chain robustness. An Institute will have an indirect impact on all of these:

*Expansion of Domestic Manufacturing Capacity:* This can be measured in several ways, such as: US percentage of manufacturing market share, amount of financial investment in manufacturing expansion, and domestic software development.

1) Market share:
    a) Domestic fab capacity: It would be better to measure actual amount of chips manufactured domestically, but since this is not practical, fab capacity can be used as a proxy
    b) Market share of domestic manufacturing both for chips and deeper in the manufacturing supply chain such as: EDA, design and development, materials, tooling, packaging, testing etc.
2) Financials: new investment in US manufacturing, US manufacturing revenue
3) Domestic software developments such as EDA, applications, and data sets

*Manufacturing Employment Expansion:* Although several factors can influence manufacturing expansion that are not directly related to employment, such as automation and product mix, manufacturing employment is a reasonable proxy for the expansion of manufacturing ecosystem. To quantify this, there are several resources that can be used to determine if – and by what rate - it is expanding. Specifically, the number of both direct and indirect semiconductor manufacturing jobs created should be considered.

*Expansion of Supply Chain Robustness:* In order to prioritize the closure of gaps in the supply chain, we must determine single sources of links in the supply chain that are manufactured outside of the US. Then, we measure how much the single-source has decreased, and either become dual-sourced or manufactured domestically. This should extend beyond simply final manufacturing steps and include what fraction of critical materials are being developed in the US as a result of developments started in the institute.

To further understand this, we envision the development of a metric which indicates the domestic content of semiconductors, similar to how the automotive industry developed a metric measuring the "US Content" of cars.

### Q28. What constitutes a successful first year for a Manufacturing USA semiconductor institute? What forms of support, and from which partners, are needed to ensure a successful first year?

Although the US is in a crisis with insufficient semiconductor manufacturing capabilities, and at risk of insufficiently supporting the supply chains of many domestic industries, we know that a thoughtfully created and operated Manufacturing Institute can help reduce risk and inspire prosperity. Despite these urgent needs, the creation of the institute should be done carefully and thoughtfully to ensure it is designed correctly. To evaluate the creation and first year of operation, several Year 1 goals should be developed to determine whether the institute is operating and functioning as intended. ***Four categories*** of start-up metrics are described below:

1) ***Membership size and diversity:*** In alignment with the mission, a good early indicator is the number of members that have joined, their financial commitments, their characteristics, and their diversity:
    - US manufacturing capabilities
    - Distribution of members across the supply chain and ecosystem including industry, academia, national labs, government, defense, and trade organizations. An excellent example of the needed diversity is the NIST-funded Microelectronics and Advanced Packaging Technology (MAPT) Roadmap[30] consisting of over 90 organizations across the ecosystem.
2) ***R&D and WFD programs launched:*** As the institute begins to operate in Year 1, a metric should include the number, sum value, and diversity of projects selected. This will also indicate that the institute has been established with an effective operational model to show that the different parts of the organization work effectively from solicitation to proposal selection, to general operation. Quantitative Year 1 metrics should include:
    - Number of students funded
    - Tech symposium training attendance
    - Training certifications earned

[30] https://www.src.org/about/nist-mapt-roadmap/

3) *Operational effectiveness and financials:* Financials are a necessary part of the institute and should be measured for Year 1. Two key metrics include:
    - Amount of committed and contracted cost-share
    - Overhead rate (<10%)
    - Operational effectiveness with the finances/ adherence to the forecasted institute budget
4) *Diversity, Equity, and Inclusion:* As DEI needs to be built into the operational model of the institute, key metrics for the first year include:
    - Number of states participating in the institute
    - Number of economically disadvantaged (Justice 40) regions represented
    - Ethnic and gender diversity of the members, performers, and institute staff

## Conclusion

We hope that the ideas, concepts, and recommendations provided in this document help NIST create a Microelectronics Manufacturing USA Institute that provides the nation and the global community with the technology needed to benefit society.