Research Needs Document: Logic and Memory Devices

June 2019

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Background

This document is prepared to accompany the Call-for-White-Papers for the research program of Logic and Memory Devices (LMD). The research needs in this area are very wide. We present here selected areas of high priorities as identified by our sponsor members.

In an integrated circuit, transistors and memories are the most important and common components. Traditionally, the main goals for scaling are density, performance, and cost. Nowadays, power, both dynamic and static, is one of the most important limiting factors to be addressed at the device level.

A new emphasis for the LMD program is on monolithic heterogeneous 3D integration that will enable greater functionality per footprint including integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics, therefore it has the potential to become a truly multi-functional platform.

For transistors, in charge-based devices, the push is for devices with lower supply voltage to generate similar current. This can be achieved by a device with alternate channel material of higher mobility or sharper turn-on characteristics (steep subthreshold slope).

The natural progression beyond the current manufacturing technologies, SOI planar MOSFETs and FinFETs, will be nanowire MOSFETs, all based on Si channel materials. Other than these Si MOSFET structures, there are potential benefits to be gained by going to other alternate channel materials with higher mobilities. It is believed that even though mobility is a low-field phenomenon, its more favorable scattering process can lead to higher high-field saturation velocity or ballistic velocity, which in turn can result in larger current or/and lower operating voltage.

Common MOSFETs encounter one common fundamental limitation of FET principle–a subthreshold slope of 60 mV/decade. This places a lower limit on the operation voltage given the required on-current to off-current ratio. Transistors that operate on the tunneling principle, rather than drift-diffusion, can provide subthreshold slope steeper than this fundamental limit. A few approaches are being examined. The common version is based on tunneling of a gate-modulated *p*-*n* junction, as in tunnel FET (TFET).

Apart from tunneling, there are other novel device concepts that can potentially out-perform conventional MOSFETs, based on additional features or different operation principles all together. One example is the internal voltage gain in NCFET (Negative Capacitance FET) which has a layer of ferroelectric as part of the gate dielectrics. Other examples in this group will be given below.

Alternate signal using spin or magnetism as a state variable rather than charge or voltage can avoid resistive power dissipation and is an attractive option. However, the propagation and logic operation based on spin, or conversion of spin back to electrical signal, is a big challenge.

The intrinsic parasitics of a logic transistor are posing multiple limitations. In particular, internal series resistance is degrading start-of-the-art CMOS device currents by more than 40%. It is also anticipated such problem will become worse with scaling. Any novel concept to improve this parasitic will improve technology of any generation.

Memories are classified into major categories of nonvolatile memories (NVMs), SRAM, and DRAM. Each has its trade-offs in different aspects of performance, its unique feature and structure, but all are critical to the industry. For NVMs, the industry has been depending on the charge-storage type, which are floating-gate FET and charge-trapping FET. However, both of these devices have a tunnel gate oxide at the channel interface, but due to the stringent requirement of long retention time, this tunnel oxide is already at its minimum thickness and is no longer scalable. Recent products have turned to 3-D to gain vertical space. The industry has started to turn to non-charge-storage types of memory cells that are typically two-terminal. For these NVMs, the critical metrics

are write/erase power, multi-bit and density, endurance and reliability, low latency, etc. The leading contenders are MRAM, PCRAM, and RRAM. More examples will be given below.

The on-state (low-resistance) characteristics of these NVM cells typically exhibit *I-V* characteristics that are too conducting at low bias, and provide leakage paths in a memory array. To control this short-coming, a selection device is needed in series. Since the memory cell is two-terminal, it is desirable to have a selection device that is also two-terminal to save space. However, a sufficient selection device that meets all of the requirements has not been fully demonstrated. Ultimately, a NVM cell with built-in selection device is the ideal solution; that is, a single NVM cell that displays *I-V* characteristics that in the low-resistance state, current is negligible at low bias.

Currently the continuing scaling of the 6-transistor SRAM cell and the 1T1C DRAM cell is experiencing formidable challenges. Lower supply voltage, demanded by lower power, causes noise margin issues. Area scaling is another big challenge. Revolutionary device concepts to realize the same functions with fewer device components would be extremely beneficial to the industry.

Research Needs

In this call, due to limited resources, we have identified topics our members have considered the most critical and relevant for university research. The list of topics are shown below, and more-detailed explanation for each follows:

1) Monolithic Heterogeneous 3D Integration using:
    - 1a) 1D Materials (CNTs & Si-/III-V-based NWs, etc.)
    - 1b) 2D Materials (Graphene, MoS2, WSe2, etc.)
    - 1c) High-electron-mobility-transistors a.k.a. HEMTs (GaN, SiC, etc.)
    - 1d) Next-Generation Spintronic MRAM (Spin-Orbit-Transfer a.k.a. SOT-MRAM)
2) Logic devices:
    - 2a) MOSFETs with high-mobility channel materials
    - 2b) Transistors based on tunneling
    - 2c) Transistors based on non-tunneling transports and phenomena
    - 2d) Transistors based on spin and magnetism
    - 2e) Functional devices
3) New concepts for contacts, junctions, and gate structures
4) Memories:
    - 4a) NVM: MRAM
    - 4b) NVM: RRAM
    - 4c) NVM: PCRAM
    - 4d) NVM: FeRAM
    - 4e) NVM: Other novel concepts
    - 4f) Analog memories
    - 4g) Revolutionary SRAM and DRAM concepts
    - 4h) Metrology for memory devices
5) Selection devices for memory arrays
6) Embedded devices
7) Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena
8) Other topics

1) Monolithic Heterogeneous 3D Integration (MH3D)

Monolithic heterogeneous 3D integration allows higher density packing and integration of logic and memory as well as mixed-signal circuits, photonics, and spintronics, therefore it has significant advantage for the development of multi-functional platform. Currently, significant progress has been made in III-V wafer bonding to 300 mm wafer sizes and hybrid Ge/III-V devices on Si. Looking further ahead, vertical Tunnel FETs, 2D materials and Spintronics are emerging as post-CMOS alternatives while continued scaling is possible with gate-all-around (GAA) and nanowire devices.

2a) Logic devices: MOSFETs with high-mobility channel materials

Many options of materials are being explored, such as different versions of III-V compounds, Si_xGe_{1-x} compounds or pure Ge, graphene, carbon nanotube, TMDs (Transition Metal Dichalcogenides such as $MoSe_2$), other 2-D and 1-D materials and structures, etc. However, the demonstration of all required specifications such as on-current, off-current, low voltage operation, etc., have to be demonstrated simultaneously. It is also important to demonstrate *n*-channel transistors with process conditions that are compatible with a high- mobility *p*-channel option (or vice versa), preferably on the same material system.

2b) Logic devices: Transistors based on tunneling

This group of devices shares the attractive feature of steep subthreshold slope beyond the fundamental limit in MOSFETs. There are many device variations in this group. The original version is TFET (Tunnel FET), where the tunnel current of a *p*-*n* junction is being modulated by the gate. Other tunneling principles involve bandgap tuning, band alignment, etc. Some versions invoke tunneling between two layers of materials separated by insulator.

2c) Logic devices: Transistors based on non-tunneling transport and phenomena

Novel logic device concepts are sought after beyond the groups 1a and 1b above. There are other kinds of working principles that are unrelated to tunneling.

2d) Logic devices: Transistors based on spin and magnetism

Transistors based on spin and magnetism to some degree. Here we include any device that involves spin and magnetism, even though charge transport as current is in some cases considered an input or output.

2e) Functional devices

Any device or structure that can duplicate a logic function performed by a network of multiple devices such as solar powered FET and others.

3) New concepts for contacts, junctions, and gate structures

New concepts to improve MOSFET structures; parasitic series resistance, abrupt junction formation, high-K/metal gate optimization, etc. Strong emphasis on novel high-K materials and junctions.

4a) NVM: MRAM

All topics related to Magnetoresistive RAM. The leading example is SOT-MRAM (Spin-Orbit-Torque MRAM). New free-layer materials and device structures (two-terminal) to lower the switching current. New reference-layer materials and tunnel barriers for high magnetoresistance.

4b) NVM: RRAM

All topics related to Resistive RAM. For example, RRAM based on motion of oxygen ions and vacancies in an oxide layer. CBRAM (conductive-bridging RAM) is a similar memory cell based on the formation of a conductive metal filament.

4c) NVM: PCRAM

All topics related to phase-change RAM.

4d) NVM: FeRAM

NVMs based on ferroelectric materials and effects.

4e) NVM: Other novel concepts

Any novel NVM cell concepts beyond that of groups 3a–3d above. Examples include electro-chemical random access memory-ECRAM utilizing redox reaction of metal ion between cathode and anode, scanning probe type memory, optic memory, etc.

4f) Analog memories
Nonvolatile memory cells that are capable of continuum equilibrium states. The challenges are controllability and reliability. They provide high density and are especially suitable for neuromorphic computing architectures. Analog nonvolatile memory elements exhibiting symmetric resistance tuning in response to pulsed inputs are particularly attractive. Problems and solutions that may arise when various new memory materials and devices operate as neuromorphic computing memory are also of interest.

4g) Revolutionary SRAM and DRAM concepts
Revolutionary concepts to realize the SRAM or DRAM functions with new materials or simpler device structures.

4h) Metrology for memory devices
Novel methods and platforms to extract memory device performance and related material characteristics.

5) Selection devices for memory arrays
A critical component for two-terminal NVM cells. Area efficiency is an important consideration in memory cell design.

6) Embedded devices
Logic or memory devices embedded in 3-D, back-end, or interconnect processes.

7) Simulations, modeling, and fundamental understanding of devices, materials, and physical phenomena
To help advancement in logic and memory devices, the use of numerical simulation is often required. In this area, we solicit ideas for improvements in modeling capabilities and in developing computationally efficient methods for materials, processes, and device operation. Use of these tools to study new material properties, unit processes, device behaviors, and quantum phenomena arising from nano-scale geometries is of high interest.

8) Other topics
Outside the six focus areas above, all submissions will be considered if containing outstanding, out-of-the-box ideas.

Reliability is a topic of interest for both logic and memory devices. Proposals addressing reliability issues pertaining to a specific device should be submitted to the group of the device type.

In this call, we encourage innovative ideas that are impactful to the semiconductor industry. Proposed work of high-risk and high-reward is especially suitable for university research.

When submitting the white papers, researchers are asked to indicate the topics (in number and sub-category such as 1c) that their research topic can best fit into.

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