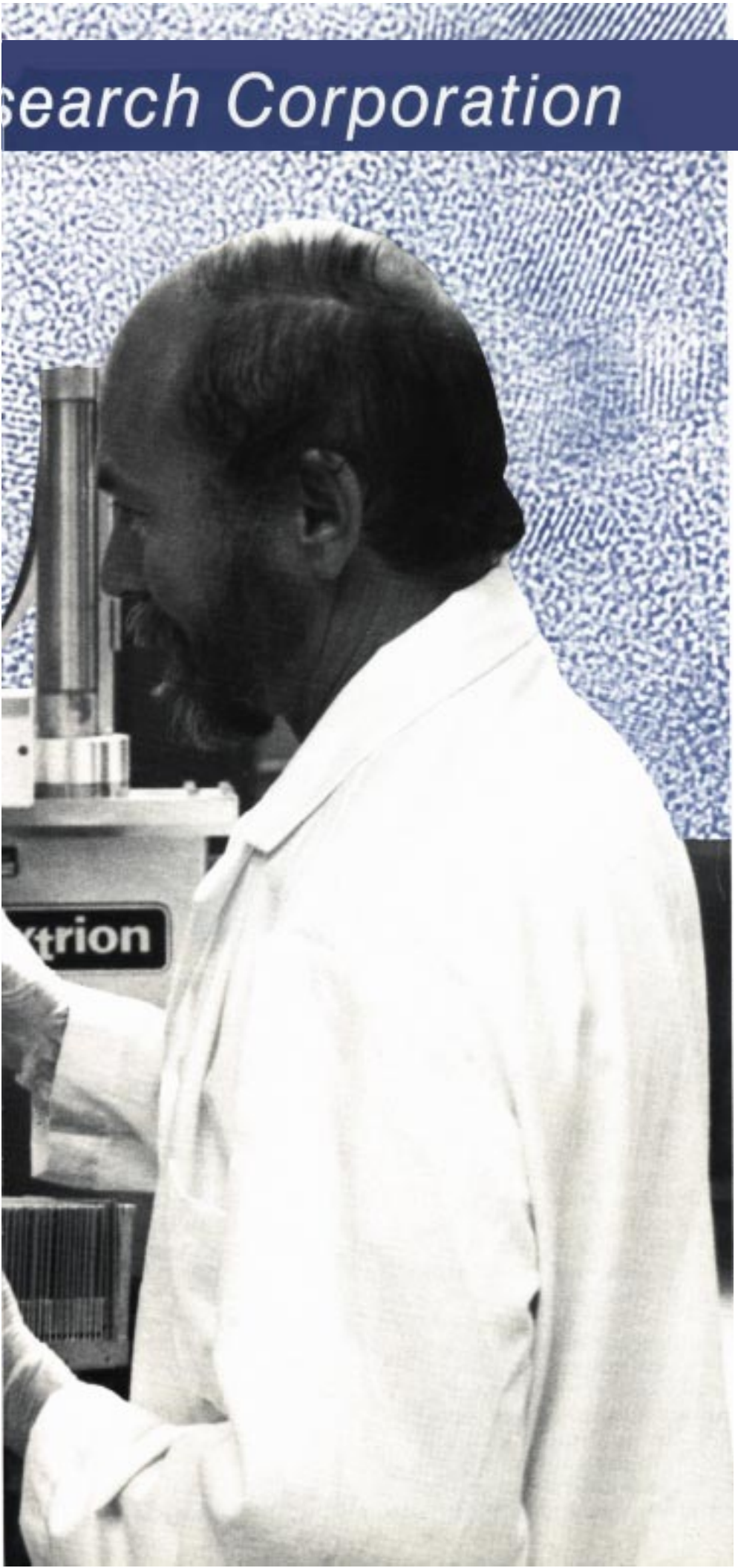
COOPERATIVE
RESEARCH

1986 Annual Report

SRC

The Semiconductor Re

search Corporation



The Semiconductor Research Corporation (SRC) is a cooperative effort of U.S. companies, with government participation, to strengthen and maintain the vitality and competitive ability of the U.S. semiconductor industry. Its purposes are carried out by a staff based in Research Triangle Park, North Carolina.

The SRC plans and implements an integrated program of basic research in university laboratories. The research has been conducted by more than 100 faculty and over 400 graduate students, and the topics selected for investigation relate to a set of long-range industry goals. During 1986, annual funding for this program's fourth year of operation exceeded $18 million.

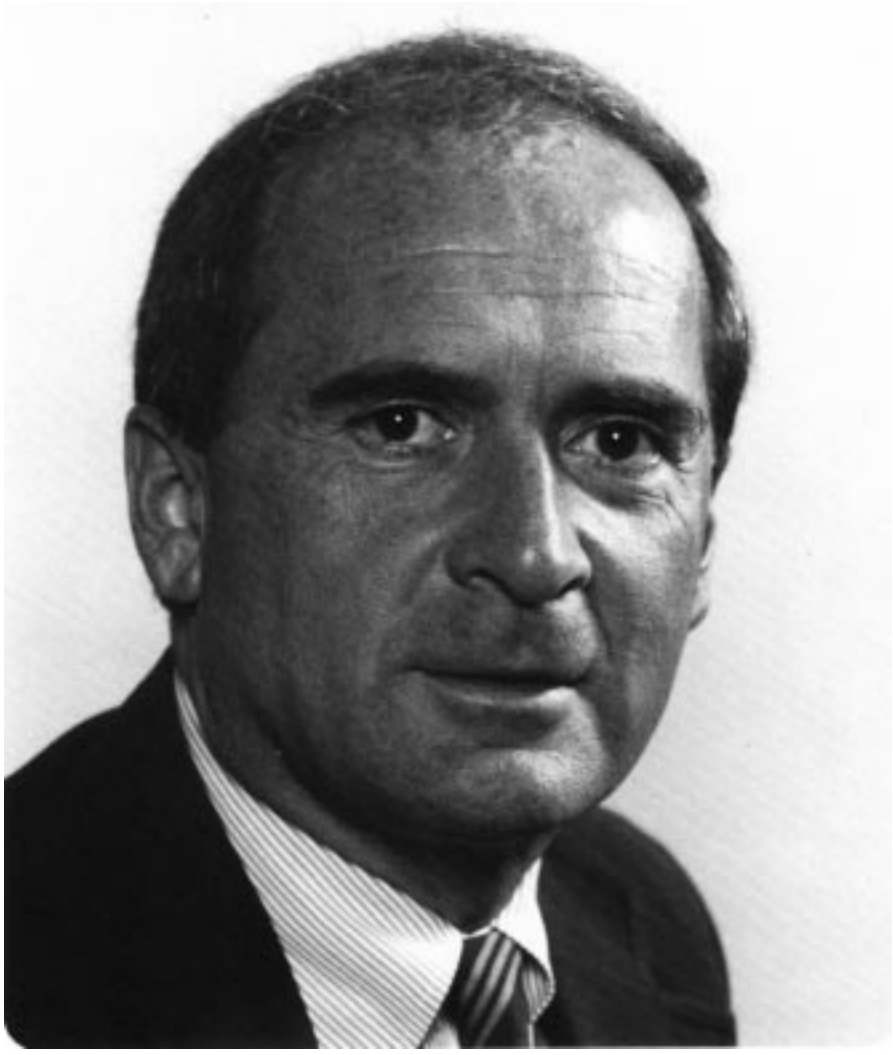
SRC research is accomplished through contracts that are closely monitored by the SRC technical staff. In addition, hundreds of staff members from the participating companies and government agencies enhance the cooperative process by their active role in advising the SRC on research coordination and planning, evaluating the SRC research program, and transferring the research results to practical applications.

The SRC's success has set the stage within the industry, and between the industry and government, to implement other cooperative initiatives that will strengthen the domestic semiconductor technology base and, thus, the competitiveness of this country in microelectronics.

Photos: FOREGROUND — Loading wafers into an ion implanter at North Carolina State University; BACKGROUND — Photomicrograph of the cross section of semi-insulating polycrystalline silicon-on-silicon produced by high resolution transmission electron microscopy.

Message

Message from the Chairman of the Board and President

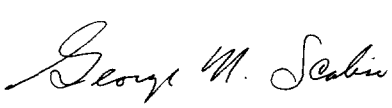


In this fourth annual report of the SRC, we are tempted to repeat those remarks introducing the first three annual reports. In the report of 1983, the SRC was declared to be a success; in 1984, we noted the major impact of the SRC in both universities and industry; and in 1985, the accomplishments of the SRC in terms of its mission were noted. Such repetition would be useful, for in each of the previously cited areas there is more to be reported. Instead, I will comment on the state of the U.S. semiconductor industry and on the role of the SRC in the industry's future.

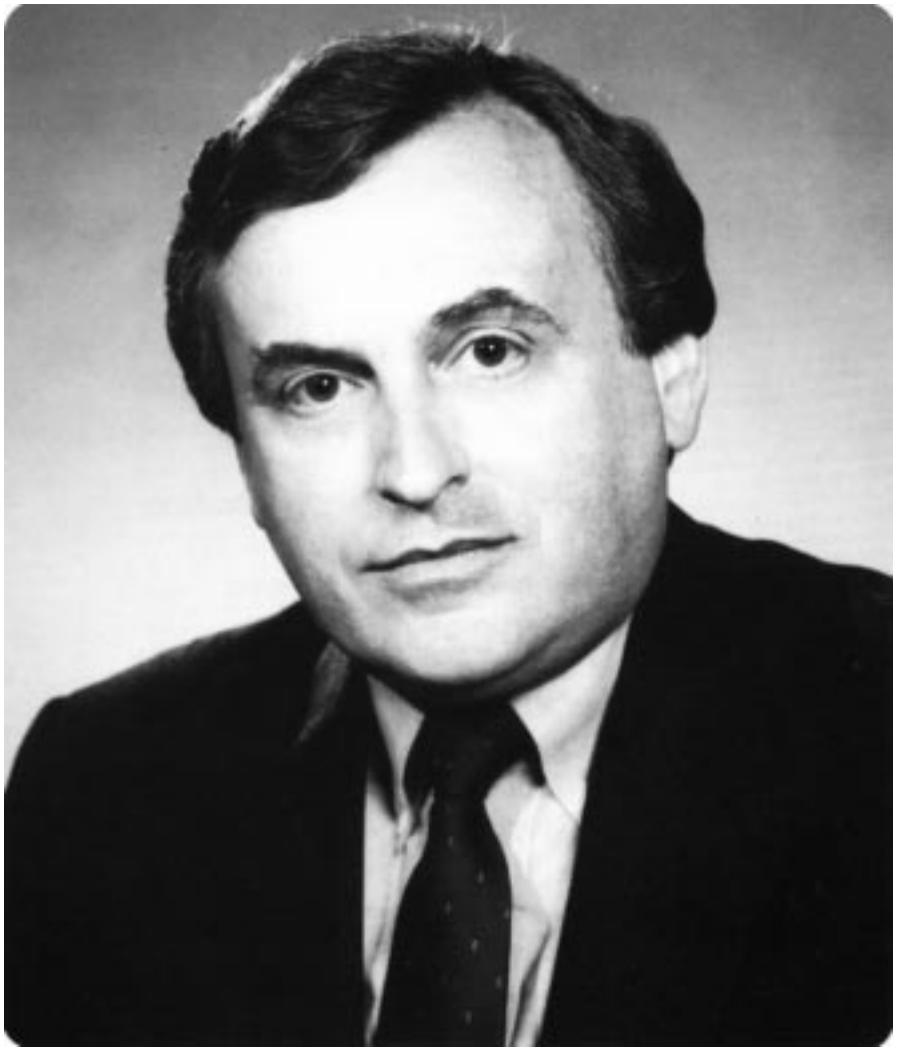
My tenure as Chairman of the Board of Directors has ended. Klaus Bowers of A T&T will succeed me. It has been a pleasure working closely with the members of the SRC board and the SRC staff for over two years. I feel that I have been part of an organization that is important to the industry, and that every person with whom I have had contact in this connection has a strong commitment to the SRC and its mission. I thank each of you for making my chairmanship both a pleasure and a success.

The winds of change are blowing strongly through the semiconductor industry. Even now, actions to forge an effective trade relationship with Japan are being taken at the highest level of government, the industry is in the process of recovering from a large excess of production capacity, new technology exchange agreements between international companies are pervading the industry, and a heightened awareness of the importance of semiconductors to the long-range national security and economic future of the United States is sweeping the halls of government. It is apparent that cooperative responses to the industry's competitiveness problems will be created and that a strategic national approach will surface in the near future.

The SRC's role in the industry is solidifying and growing. I have asked Larry Sumney in his comments to address this issue in more depth. I believe that the seeds of cooperation which have been successfully nurtured in the SRC will expand beyond generic research, and that the SRC, as the springboard of cooperation in semiconductor technology, will play an increasingly important role in this expansion. All of us participating in the SRC will derive satisfaction from having been part of these changes.



George M. Scalise
Chairman, Board of Directors



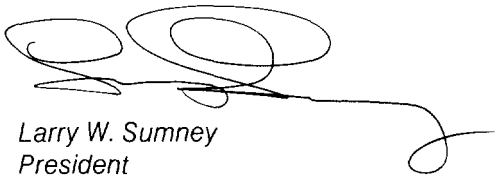
At the SRC's inception, the founders defined its mission to be generic research and the education of skilled manpower for the semiconductor industry of the United States. In its response to this mission, the SRC has built a strong integrated research program that involves meetings of industry and university research representa fives in many technical areas for planning the direction and goals, evaluating progress, and assessing the results. These forums have provided unique views of the technical agenda of the U.S. semiconductor industry. For example, the SRC has established for the industry 10-year goals, which are supported by its research, and is in the course of evolving a research roadmap. This roadmap will apply not just to the activities of the SRC but to all elements of the U.S. research community that support these goals.

Because the SRC's research mission requires planning and assessment of technology on behalf of the industry, it has become a de facto source of industry plans with respect to semiconductor technology. In this role, the SRC has become involved in addressing needs of the industry beyondits generic research mission. An example is the activity of the Manufacturing Competitiveness Panel (MCP) which is an outgrowth of the Manufacturing Sciences Program. The MCP began because of the recognition that broader issues in manufacturing must be addressed in order to provide a rational response to industry needs. The long-range plan of the SRC includes recognition of this expanded role by initiating industry support activities beyond the scope of the generic research and education missions.

What does this mean? First, the SRC must view its research as one part of a national semiconductor strategy and integrated with the government and industry efforts with which it interfaces. Second, the SRC may be called upon to provide integrated research support for other cooperative activities such as SEMATECH with resultant impacts on its program. Third, it is important that the SRC participate in the formulation of the various components of a national strategy so as to provide an amalgamated industry input, particularly to the research components of this strategy. Finally, through interactions with its members, the SRC must identify needs and priorities that best represent the industry rather than any one company or industry sector.

In undertaking this expanded role, the importance of the original mission must not be lost. Generic research is, and will continue to be, the central mission of the SRC. However, since a national semiconductor strategy is very important to the industry and its ability to compete, the SRC has a responsibility to provide whatever help it can in creating such a strategy. We hope that our efforts will result in the identification and creation of mechanisms for addressing broad technology questions As these changes in the semiconductor technology base of the U.S. occur, whatever their form, I foresee an expansion of the SRC, both in its funding for generic research and in its representing the technology of the industry.

As always, when I refer to the SRC, I include not just the small corporate staff, but also the industry/government representatives who combine their efforts and cooperation to make the SRC work and ensure its success, and the faculty and students who perform the research for which the SRC exists. Collectively, we are the SRC.



Larry W. Sumney
President

Participants

Companies

AT&T
Advanced Micro Devices, Incorporated
Applied Materials, Incorporated
Burroughs Corporation
Control Data Corporation
Digital Equipment Corporation
E.I. du Pont de Nemours & Company
E-Systems, Incorporated
Eastman Kodak Company
Eaton Corporation
G CA Corporation
GTE Laboratories, Incorporated
General Electric Company
General Motors Corporation
Goodyear Aerospace Corporation
Harris Corporation
Hewlett-Packard Company
Honeywell Incorporated
IBM Corporation
Intel Corporation
Monolithic Memories, Incorporated
Monsanto Company
Motorola, Incorporated
National Semiconductor Corporation
The Perkin-Elmer Corporation
RCA Corporation
Rockwell International Corporation
SEMI, Chapter
Silicon Systems, Incorporated
Sperry Corporation
Texas Instruments Incorporated
Union Carbide Corporation
Varian Associates, Incorporated
Westinghouse Electric Corporation
Xerox Corporation

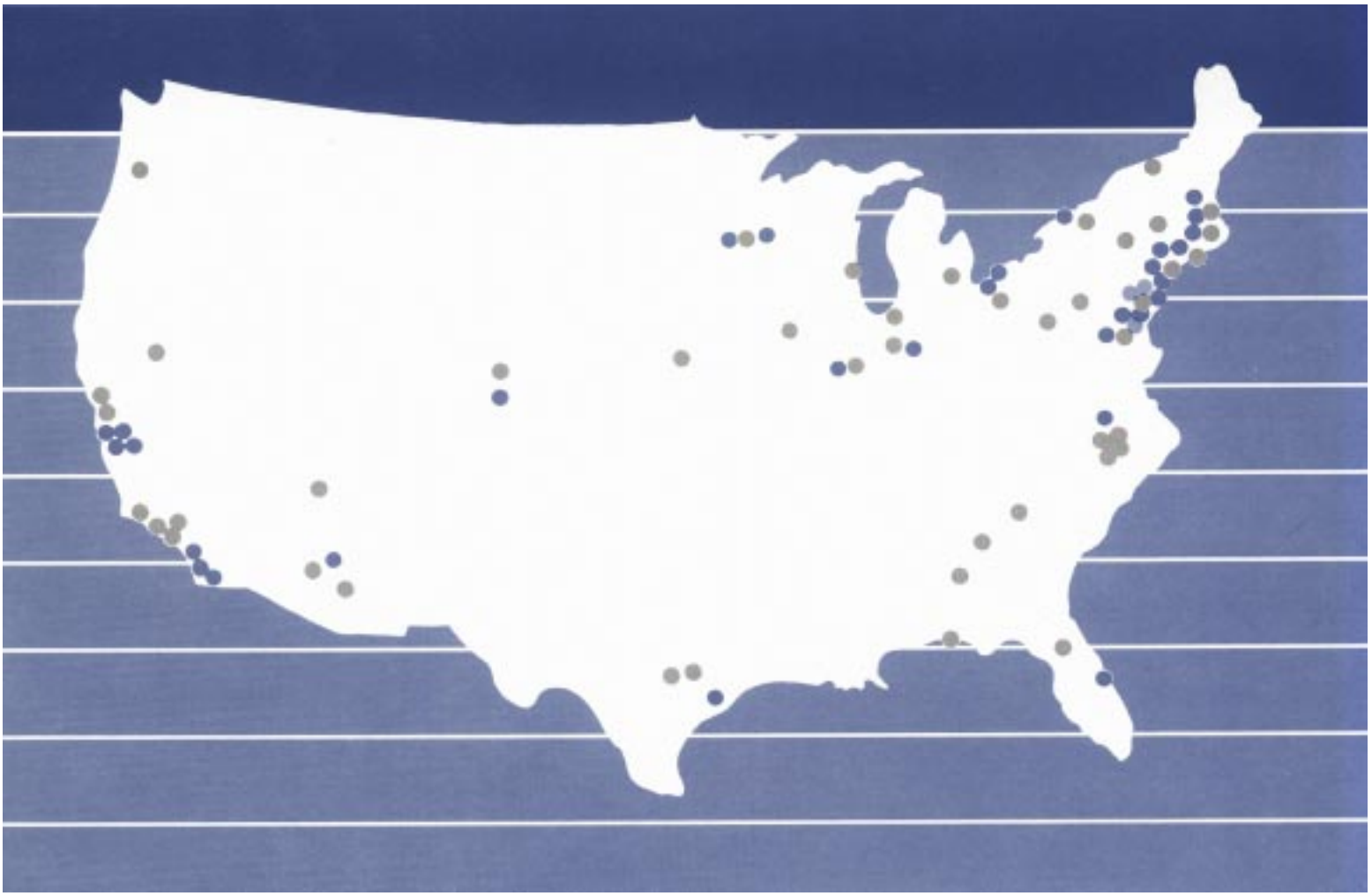
*The following companies are included in the Semiconductor Equipment and Materials Institute, Inc., CHAPTER:

ASYST Technologies, Inc.
Dynapert/Amedyne
Eagle-Picher Industries, Inc.
Emergent Technologies Corporation
FEP Analytic
FSI Corporation
Genus, Inc.
Gryphon Products
Hercules Specialty Chemicals Company
Ion Beam Technologies, Inc.
Ion Implant Services
Lehighton Electronics, Inc.
Logical Solutions Technology, Inc.
MacDermid, Inc.
Machine Intelligence Corporation
Machine Technology, Inc.
MG Industries/Scientific Gases
Micrion Corporation
The Micromanipulator Company, Inc.
Micronix Corporation
Oneac Corporation
Optical Specialties, Inc.
PT Analytic, Inc.
Pacific Western Systems, Inc.
Peak Systems, Inc.
Sage Enterprises, Inc.
The SEMI Group, Inc.
Silsco, Inc.
Solid State Equipment Corporation
Thermco Systems, Inc.
UTI Instruments Company
VLSI Standards, inc.
XMR, Inc.

**The commitment for individual participation by these companies in the SRC preceded corporate mergers that took place in 1986.

Government

Department of Defense
National Science Foundation
National Security Agency



Institutions

Arizona, University of
Arizona State University
Auburn University
Brown University
California at Berkeley, University of
California at Los Angeles, University of
California at Santa Barbara, University of
California Institute of Technology
Carnegie-Mellon University
Case Western Reserve University
Clemson University
Colorado State University
Columbia University
Cornell University
Duke University
Florida, University of
Florida State University
Georgia Institute of Technology
Illinois at Urbana/Champaign, University of
Iowa, University of
The Johns Hopkins University
Lehigh University
Massachusetts Institute of Technology
Michigan, University of
Microelectronics Center of North Carolina
Minnesota, University of
Nebraska at Lincoln, University of
North Carolina at Chapel Hill, University of
North Carolina State University
Notre Dame, University of
Oregon Graduate Center
The Pennsylvania State University
Purdue University
Rensselaer Polytechnic Institute
Research Triangle Institute
Rochester, University of
Southern California, University of
Stanford University
Texas at Austin, University of
The Texas A&M University
Vermont, University of
Wisconsin, University of
Yale University

Cooperation

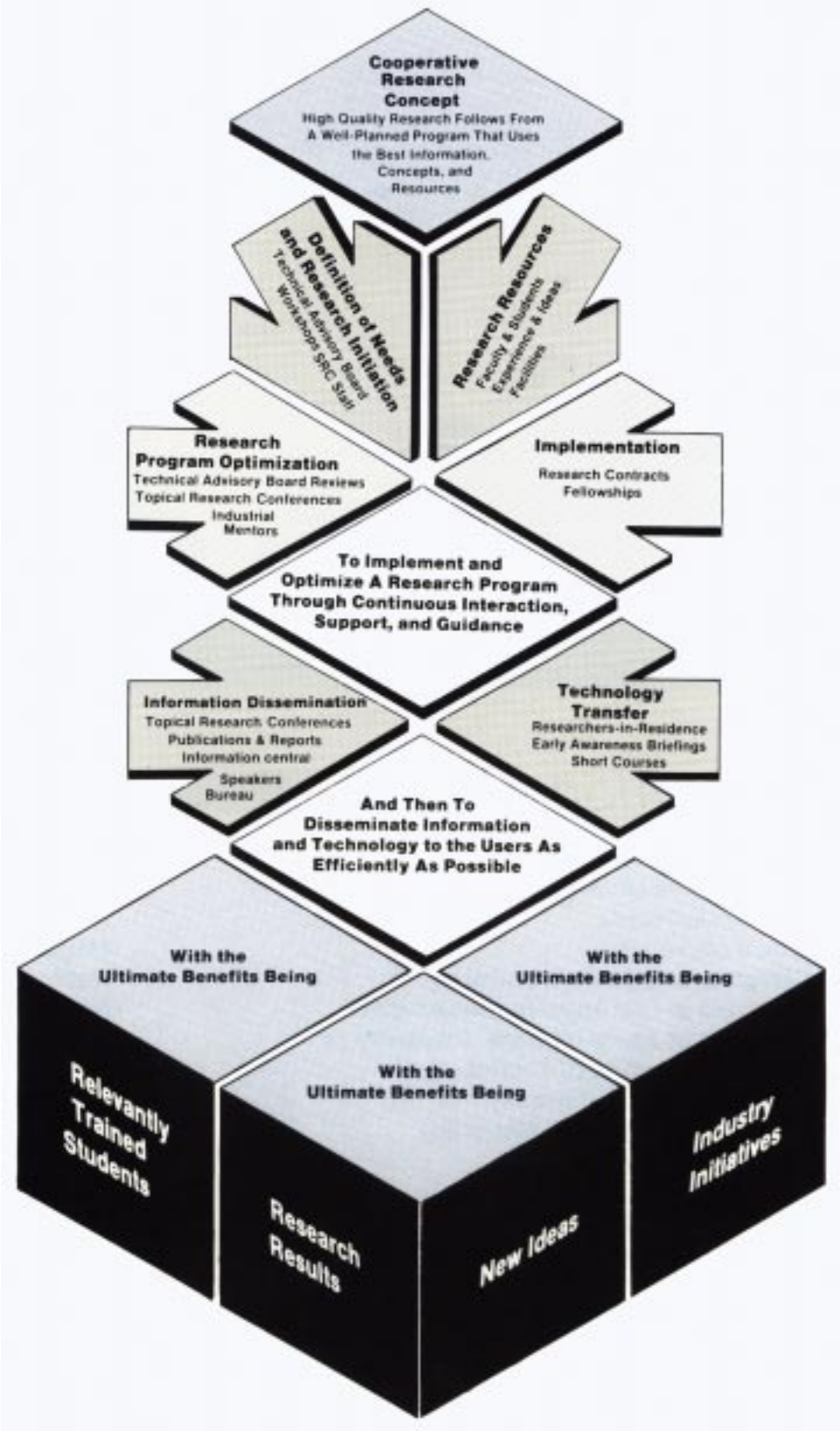
Mission

Toward the end of the 1970s, trends began to indicate that the U.S. was losing the comfortable margin of world leadership in microelectronics technology and the ability to compete successfully for domestic and international markets which it had enjoyed since the invention of the transistor four decades earlier. In response to these trends, eleven companies with an interest in integrated circuits formed the SRC in 1982 as a nonprofit organization through which they could cooperate to maintain the vitality and competitiveness of the U.S. semiconductor industry.

Two priorities were identified for the SRC's initial mission: establishing an efficient program of basic research to accelerate growth of the technology base for the semiconductor industry, and increasing the supply of well-educated manpower for the industry.

In response to this mission, activities of the SRC during the first four years of operation have centered around planning and implementing an integrated program of cooperative research that is conducted at already existing research facilities on the campuses of U.S. universities. Since 1982, the SRC has directed cumulative funding in excess of $60 million to the support of this research.

In 1986, the Board of Directors expanded the mission in recognition of a role for the SRC in responding to a broader set of industry needs. These are referred to as Industry Support Activities and include expansion of the cooperative concept, industry interactions, and integration with complementary research programs.



Support and Guidance

The SRC addresses its assigned mission by:

- *using as input the resources, both financial and manpower, made available by the industry and government participants, and*
- *providing as output the research results from the universities, graduates that enter the university manpowerpools, and the products of its Industry Support Activities.*

Thirty-five companies provided funding for the SRC in 1986, including a chapter member that is an association of thirty-three small equipment and materials suppliers. Beginning in September of 1986, three agencies of the Federal Government became SRC participants through a Memorandum of Understanding between the SRC and the National Science Foundation.

The industry and government participants also contribute thousands of man-hours by hundreds of staff members to advise the SRC on the selection of research initiatives; to establish relevancy of the research to the needs of the industry; and to transfer new technology from the university laboratories to industry for testing, development, and practical application.

THE BOARD OF DIRECTORS is the SRC's policymaking body; and during 1986, the voting membership included 16 representatives from member companies and the President of the SRC.

THE TECHNICAL ADVISORY BOARD (TAB) is the SRC's major research advisory group and the prime technical interface to the staff of the funding participants (see membership roster on pages 34-35). The TAB Executive Committee addresses global issues and coordinates the activities of the three technical committees that deal with the separate science areas of the research program. In 1986, the Executive Committee formed subcommittees on technology transfer, invention review, integration of long-range research roadmaps, and the evaluation of research projects. The TAB technical committees review research proposals for new funding, participate in evaluation of ongoing research contracts, and annually review each component of the overall research program for continuing relevance, quality, and productivity, and advise the SRC on appropriate actions.

INDUSTRIAL MENTORS are scientists or engineers from member companies who maintain an active, constructive interface with principal SRC faculty researchers. By the end of the 1986 calendar year, 280 mentors from 41 companies were assigned. The mentors advise the university research teams on industry knowledge, consult on research techniques, and highlight significant new technology. Each year a survey of the mentors and their respective faculty investigators is conducted to evaluate the quality of the Mentor Program, record the interactions that have occurred, and list technologies being accessed by member companies. Significant positive interactions have been reported, ranging from donations of research equipment to instances of the co-authoring of papers by mentors and university professors.

INDUSTRIAL RESIDENTS are employees of member companies who join the SRC technical staff for periods of one to two years. As members of the staff, the residents provide industry perspective to the research program and participate in monitoring the research contracts. Having an employee on site for continuous access to the research is an excellent mechanism for maximizing technology transfer.

The SRC STAFF in 1986 consisted of 28 professional and support personnel—including three industry residents, who provided coordination, management, and continuity to the cooperative effort. Ten members of this staff were assigned to management of the research program, four to technology transfer, three to operation of the computer-based information system, and the remainder to administration and general operations.

Information Dissemination

A variety of SRC initiatives and ongoing events facilitate technology transfer among SRC participants from industry, government, and universities; among universities; and among member companies.

WORKSHOPS are the mechanisms for gaining a broad perspective on a specific technical area that is being considered as a research initiative. Experienced scientists and engineers are invited from industry, government, and academia to explore the feasibility and advisability of pursuing the suggested initiative. In 1986, the SRC conducted two workshops: Software Portability to address issues of software technology transfer from university to industry, and Computer-Integrated Manufacturing architecture and implementation.

TOPICAL RESEARCH CONFERENCES (TRCs) are conducted on university campuses to foster active dialog among SRC researchers from industry, government, and universities on a specific technical topic. A unique forum for cooperation, the conferences serve as a vehicle for early access to research results, input from unpublished industrial research efforts, and constructive criticism of the research area. During 1986, four TRCs were conducted:

- *Bipolar Device Technology at Arizona State,*
- *Manufacturing Sciences at Stanford,*
- *Packaging at Lehigh, and*
- *Quarter-Micron CMOS Technology, Part II, at UCLA.*

EARLY AWARENESS TECHNICAL BRIEFINGS (EATBs) are held on university campuses to present a priority review of a recent invention or technical breakthrough. These briefings can be important in an industry where timeliness is a major competitive asset. Two briefings, In Situ Laser Processing at Stanford and The Automatic Synthesis Project at UC/Berkeley, were presented in 1986.

TECHNOLOGY TRANSFER COURSES (TTCs) are conducted on university campuses to provide staff from member companies the opportunity for hands-on experience with a new technology in the university laboratory. Particularly in the case of software and analytical techniques, a direct transition can be made from university research to industrial use. Taught by university researchers, Technology Transfer Courses have proved very popular. The courses taught in 1986 were:

- *Advanced III-V and Silicon Device Modeling at Purdue,*
- *AIDE2.1: An Analog CAD Package at Georgia Tech,*
- *Kinetic modeling of Directional Plasma-Etching Processes at MIT,*
- *Process Modeling with SUPREM, SAMPLE, and SIMPL at UC/Berkeley,*
- *CHIEFS at Illinois Urbana/Champaign,*
- *GaAs HEMT Device Models at Stanford,*
- *FABRICS at Carnegie-Mellon,*
- *Microstructures: Characterization and E-Beam Lithography at Cornell.*

INFORMATION DISSEMINATION takes a variety of forms in order to serve the diverse needs of the SRC community.

The SRC library now contains over 2200 publications generated from university research and by staff of the SRC in addition to several video tapes that are available to member companies and research investigators. The number of publication requests has risen to over 1000 a month.

information Central is the SRC's computer-based information/communication system that operates on a 24-hour basis and accommodates electronic mail, requests for publications, and event registration for over 300 remote and local users. In 1986, the research abstract database was made more accessible by the implementation of a new keyword search capability that has increased usage dramatically.

The monthly SRC Newsletter reached a circulation of 3600 by the end of 1986.

FABRICS Technology Transfer Course at Carnegie-Mellon

Research and Education

The environment of the universities in semiconductor research varies from a small number of very strong institutions with large facility investments and strong and diverse faculties, to smaller schools with several faculty members and minimal facilities, attempting, with difficulty, to maintain a productive research niche. The spread between the top and bottom is very large, and it is not unusual to find university efforts compartmented in such a manner that monodisciplinary attitudes prevail.

In this environment, the SRC is attempting to bring together teams of researchers, to raise the performance capabilities of second-tier schools, to initiate research in nontraditional disciplines, and to orient the research efforts toward goals defined on the basis of needs.

The SRC provides a cooperatively defined window on the future of semiconductor technology. This window results from planning and forecasting of technology trends, particularly as affected by competition, andprovides a set of goals and objectives for the industry that must be supported by SRC-funded university research.

The role of the universities is to explore the nature of the various approaches for achieving these objectives through research that provides knowledge on materials, processes, phenomena, structures, and devices; on the hierarchy of design too/s and approaches for advanced integrated circuits and systems; and on the methodology employed in fabricating these designs and delivering them as competitive products to customers. Contributions to this knowledge base, characterized by the creativity and innovation that exist in the multidisciplinary environment of the university, are the function of SRC research.

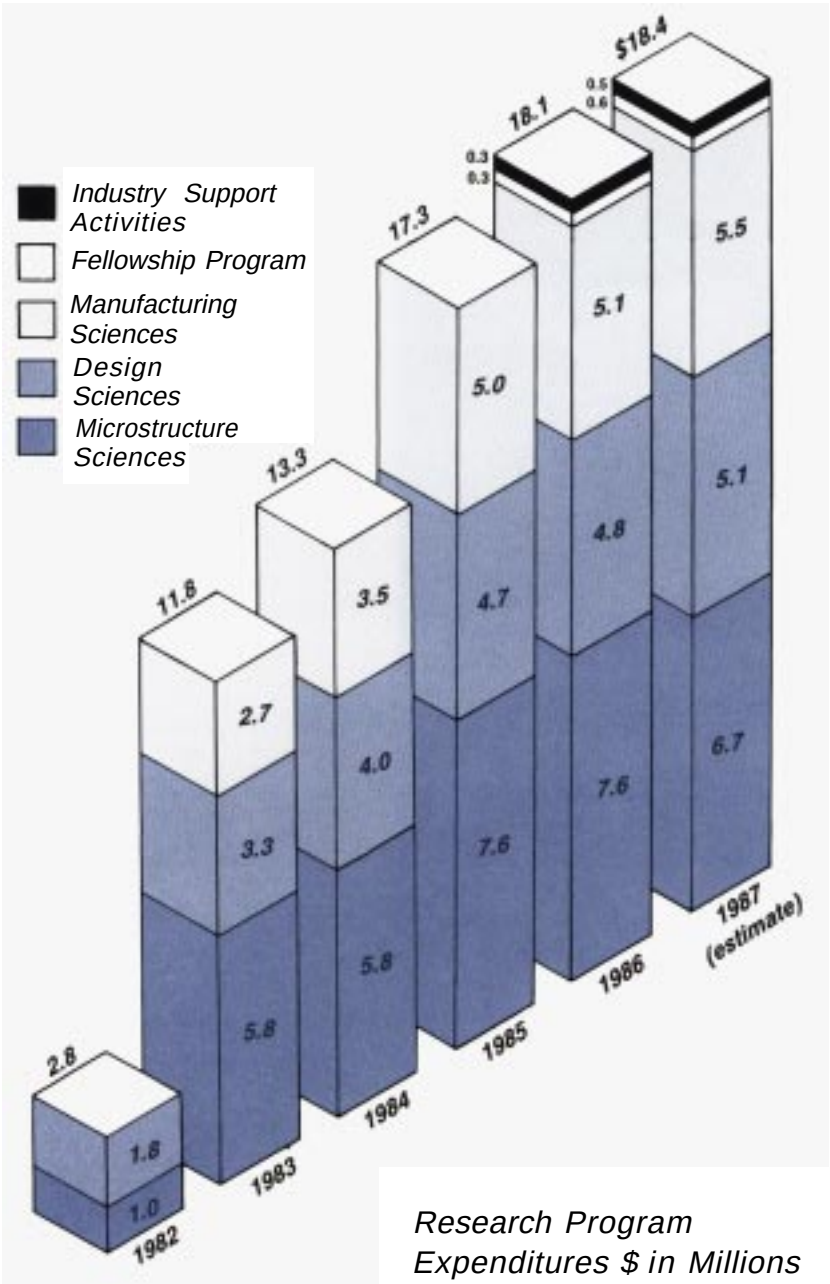
THE SRC FELLOWSHIP PROGRAM began support in the fall of 1986 for 19 graduate students seeking advanced degrees in microelectronics. The goal of this program is to increase graduate student support (beyond that already going to graduate students associated with SRC contracts) in the specific areas of microelectronics that are of most interest to SRC companies. Research in which fellowship recipients participate is directed by SRC investigators.

SRC Fellow James Comfort with plasma-enhanced epitaxial silicon reactor in the new clean room at MIT. (See "Low-Temperature Epitaxy" research highlight on page 12.)

THE SRC UNIVERSITY ADVISORY COMMITTEE (UAC) is an independent body of university faculty that meets twice a year, including an annual meeting with the SRC Board of Directors and TAB, to give counsel on issues relative to the university community. This body has an important role in establishing policy for the research program. (See membership roster on page 34.)

Science Areas

The science areas around which the SRC is organized — design, manufacturing, and microstructure — were identified early in its history as the best structure with which to relate to the industry and the universities. The science areas overlap in their activities, and each is strongly connected to the others through the research thrusts and the technology vehicles, These science areas provide unified responses to the 1994 research goals that are focused on complexity, functionality, reliability, and cost. In brief, these goals are to make possible in 1994 the prototype production of chips with (1) 250 times the complexity of those available in 1984 (equivalent to a 256 Mbit DRAM), (2) functional throughput rates of 5 x 10^{15} gate-hertz, (3) a reliability such that less than 10 failures occur in 1 billion operating hours of an integrated circuit, and (4) a 500-times reduction in cost per functional element relative to that in 1984.

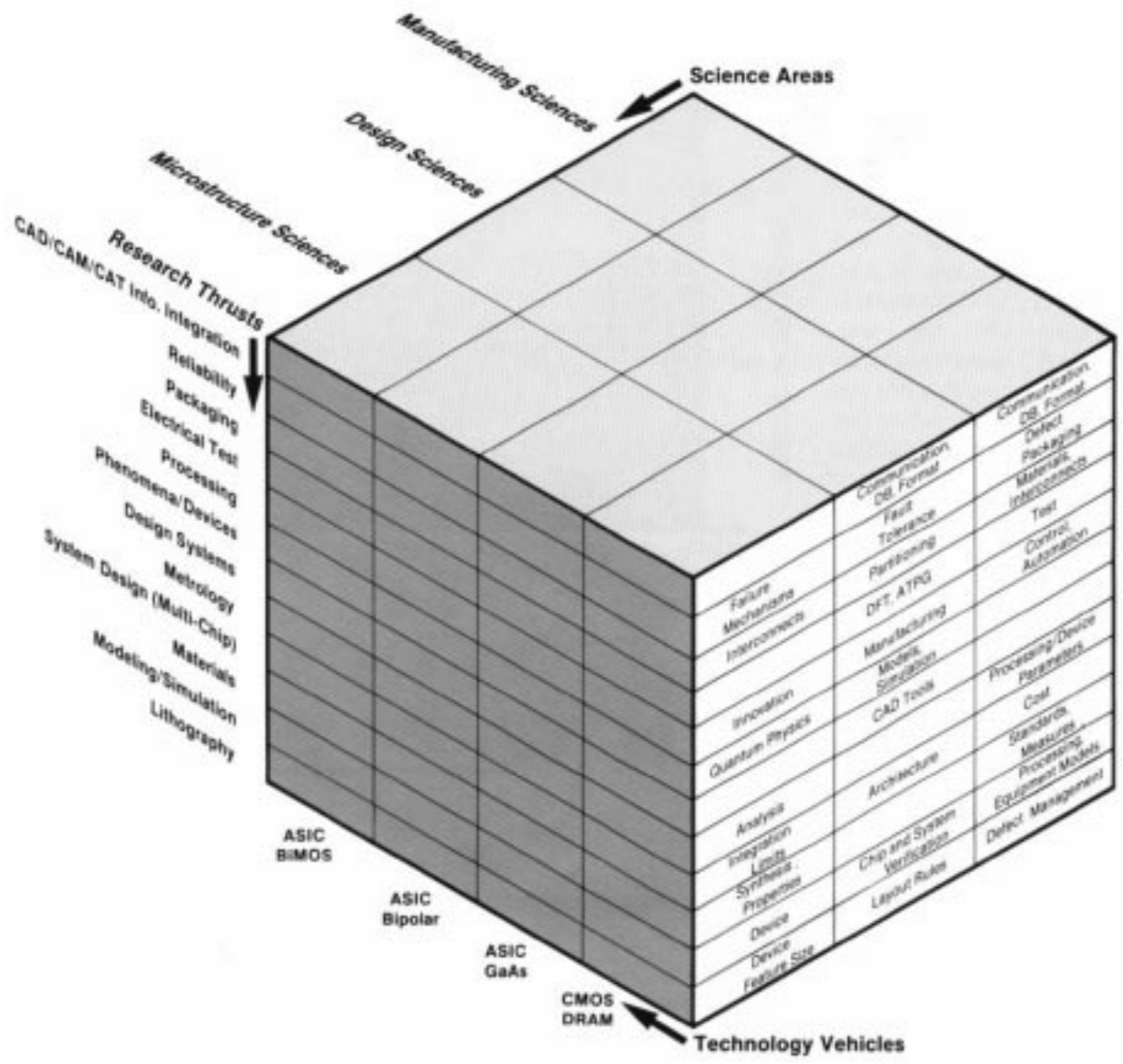


Research Program Expenditures $ in Millions

The DESIGN SCIENCES area includes coordinated efforts in system synthesis and verification, design for testability and reliability, design system integration, linear integrated circuits, process and device modeling, physical design, and VLSI architectures. The objective is to enable the development of design systems by SRC members that support the rapid design of manufacturable IC systems which achieve specified levels of quality and performance. The Design Sciences area is characterized by a high degree of productivity as measured by the number of design software packages being produced and transferred to SRC members, and by the level of scholarly achievement.

The MANUFACTURING SCIENCES area deals with the quantification, control, and understanding of the semiconductor manufacturing processes necessary to achieve a predictable and profitable product output. Research is directed to quality, productivity, cost, packaging, CAD/CAM/CAT, and reliability. Efforts in 1986 addressed computer-aided manufacturing and advanced processing technologies, automation, yield enhancement and reliability, packaging, metrology, and curricula for the education of manufacturing-oriented engineers.

The MICROSTRUCTURE SCIENCES area is concerned with the phenomena, materials, and processes used to fabricate semiconductor devices, and the integration of these devices into VLSI circuits. Five principal thrusts are being addressed: 0.25 micron CMOS, in situ processing, bipolar technology, gallium arsenide integrated circuits, and quantum devices. The goal of this area is to accelerate the technology for industry members by 1994 that will lead to logic and memory capability levels corresponding to 40 x 10^6 and 200 x 10^6 transistors per sq cm, respectively,. a switching delay of 50 picoseconds; and a power delay product of 5 femtojoules per gate.



Research Planning

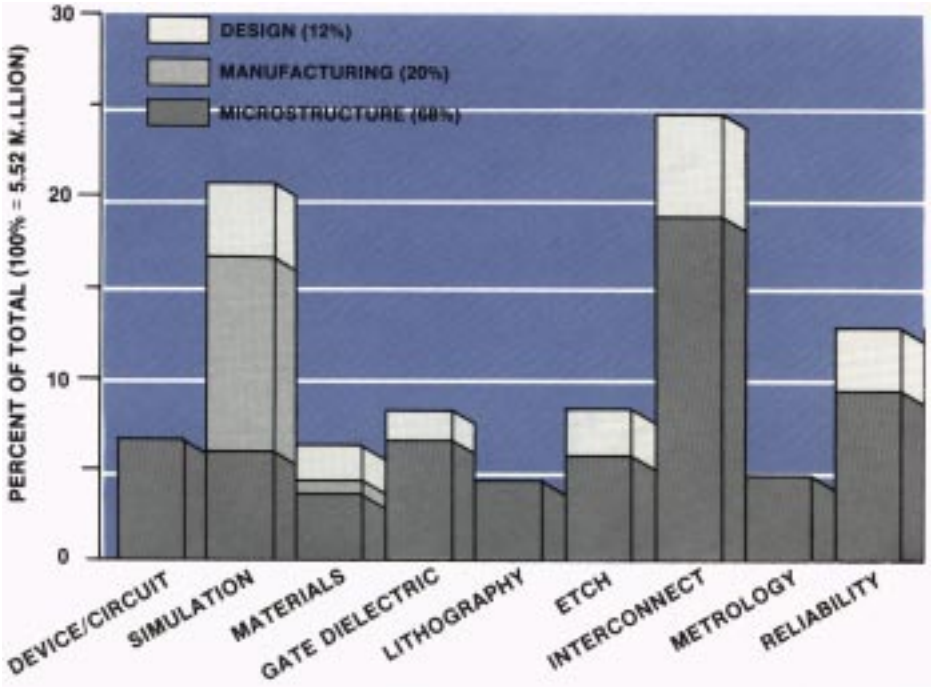
The research activities of the SRC, for *planning purposes, are viewed in three dimensions..*

- *TECHNOLOGY VEHICLES that employ the characteristics of future integated circuit products to define* goals *for the SRC,*
- *RESEARCH THRUSTS that are the areas of study involved in the realization of all of the technology vehicles, and*
- *SCIENCE AREAS that are discipline-based and* are *used to provide a management structure consistent with that of the industry and universities.*

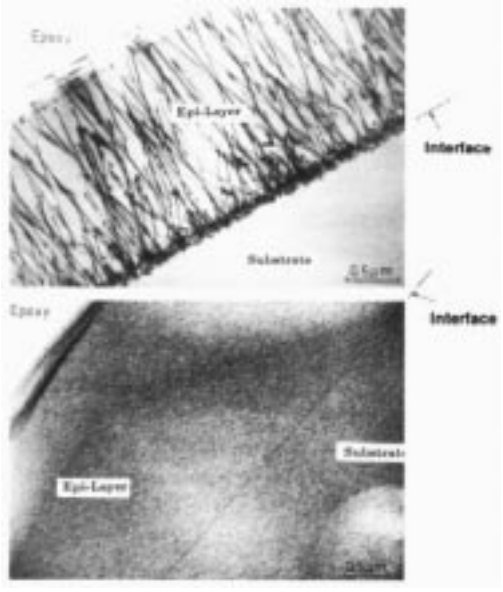
The cells in the space defined by these three dimensions contain the specific task, contribution, or objective in each science area for each research thrust associated with each technology vehicle. Some cells are empty while other represent large efforts of the existing program. Exploratory SRC research is also *underway that does not map into this planning matrix. Exploratory research will continue to be an important part of the program.*

CMOS and BiCMOS Technology

The achievement of a 0.25 micron low-power, high-performance device/circuit and fabrication CMOS and BiCMOS technology is a key accomplishment of the SRC industry-established goals for 1994. About one-third of the total SRC research effort is directed to investigations that are significant to achieving this objective, which is believed to be at the practical scaling limit of MOSFETs. The principal research projects are being performed at the SRC Centers of Excellence and Programs at the University of California at Berkeley, Cornell University, Carnegie-Mellon University, and the Massachusetts institute of Technology, aided by individual projects at a large number of additional universities. This research thrust is coordinated by the elements shown in the figure entitled, "One-Quarter Micron CMOS Strategy."



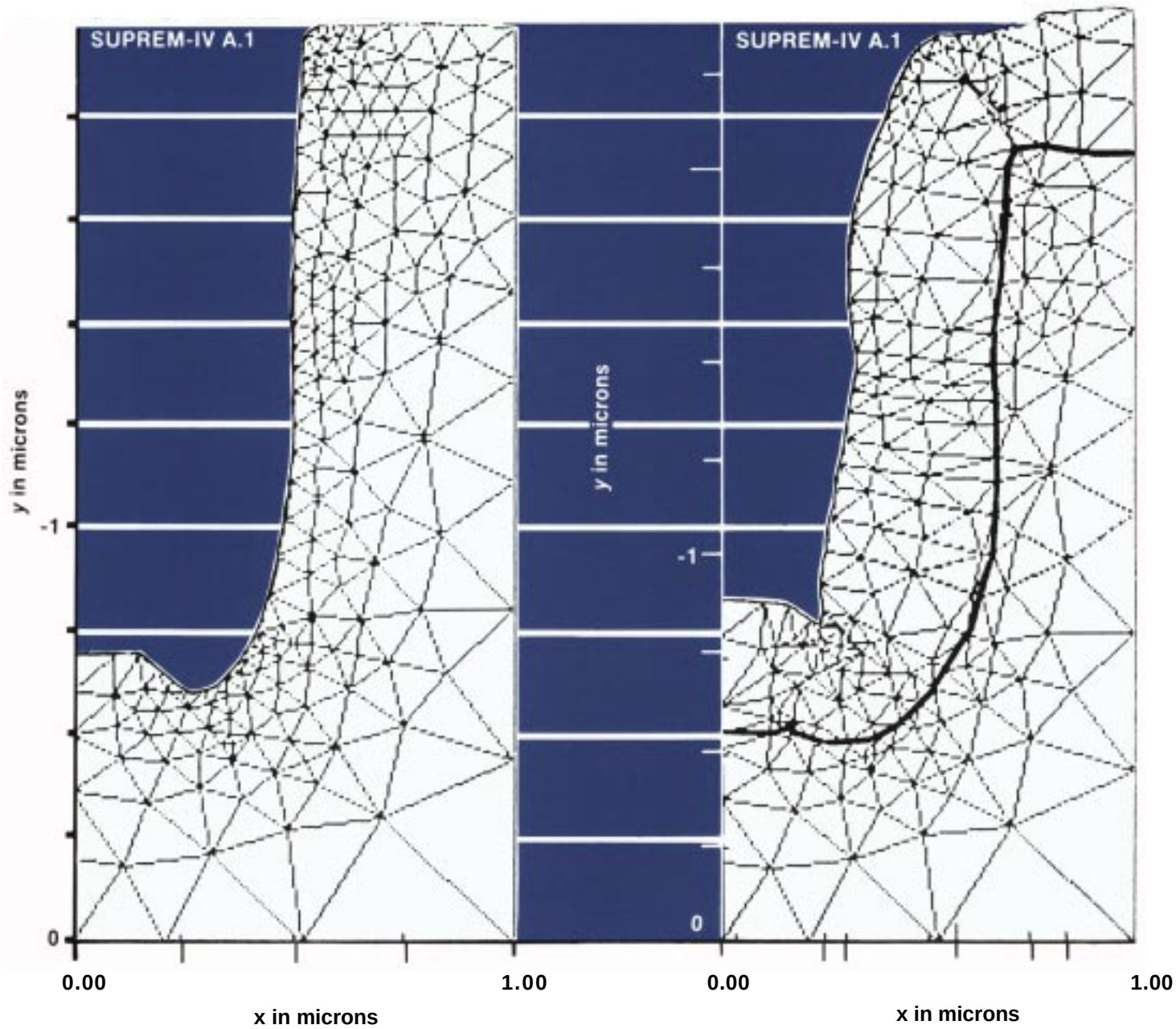
One-Quarter Micron CMOS Strategy



Low Temperature Epitaxy

Low temperature processes are essential to the development of 0.25 micron CMOS circuits. In particular, epitaxial silicon deposition temperatures must be reduced from the 1050°C to 1250°C levels conventionally employed to below 800°C to control dopant redistribution on a submicron scale while not allowing a corresponding degradation of the material quality. The critical step in the deposition of high quality epitaxial silicon is the in situ surface clean preceding the deposition. Under the SRC/MIT Program, "Novel Processing Technologies for Silicon Integrated Circuits," researchers have developed an in situ low-energy argon sputter cleaning process to remove native oxide from a silicon surface without introducing permanent damage. The process exploits enhanced sputter efficiencies observed for silicon and silicon dioxide above 600°C, and has been implemented in a unique plasma-enhanced deposition reactor for low temperature silicon epitaxial deposition. The cross-sectional micrographs made by transmission electron microscopy (TEM), which are shown in the accompanying figure, dramatically illustrate the results of this technique. The upper TEM image shows heavily dislocated epitaxial deposits at 750°C, following a high-energy sputter clean. The lower TEM image shows a dislocation-free film obtained using a low-energy process.

Professor L. Rafael Reif
Massachusetts Institute of Technology



Grid Structure (left) and the Final Oxide Shape (right) on a Trenched Surface, Simulated Using SUPREM-IV A

Process Simulation

The development of VLSI processes is becoming more complex owing to both reduced device dimensions and the strong dependence of these dimensions on surface physics, e.g., stress-dependent oxide growth and the effects of point defects on dopant diffusion are both highly two-dimensional. In this research project, SUPREM-IV A has been used for process simulations such as that in the accompanying figures which show the grid structure and final oxide shape on a trenched surface. Based on the stress-dependent oxidation model of Kao, et al. (IEDM, 1985), the simulations accurately predict thinning at both convex and concave corners. Beyond the two-dimensional effects given by using SUPREM-IV A, the problems of three-dimensional device structures are of growing importance. For example, trenches are being used for both storage capacitors (DRAMS) and for isolation. Preliminary results of 3D oxidations simulations have been achieved through the Stanford process simulation efforts, and future investigations willcontinue to explore and characterize both the physical coefficients and simulation tools for developing advanced 2D and 3D structures.

Professors J.D. Plummer and R.W. Dutton
Stanford University

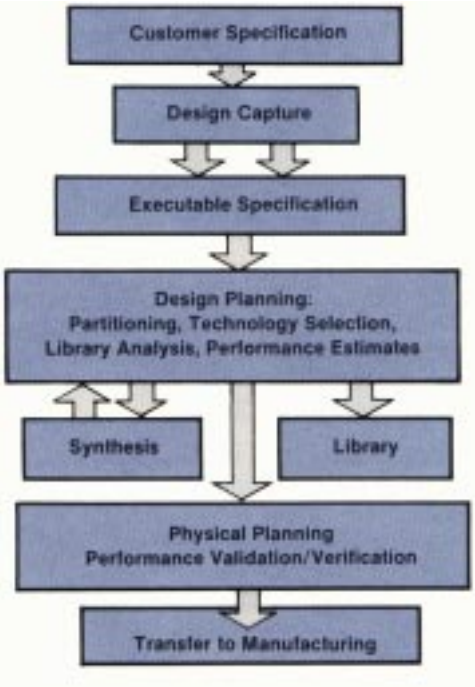
Design Systems

The design of complex integrated circuits and chips requires the utilization of design systems rather than stand-alone sets of design tools. Design systems provide an environment for the linkage of collections of tools, the underlying data management systems, and support for a well-defined user interface. Moreover, the design system should provide a target set of specifications for the development of new or additional tools.

Because of the geographical distribution of the universities involved in the conduct of SRC research and the diverse end-use community for the research results, it has become necessary for the SRC to take action to develop guidelines for the university researchers to use in the development of software tools. As the result of a Workshop on Software Portability conducted by the SRC in 1986, software development guidelines are being established for use by university researchers. The focus of the effort emphasizes the definition and use of software engineering principles such as modularity, clearly identified input/output sections of code, and clearly defined machine-dependent parameters rather than the specification of a specific language or operating system by university researchers, although UNIX and C predominate. A second emphasis is on the use of graphics standards, such as GKS, and widely accepted window managers like X-Windows. To the extent possible, the SRC will support the use by research teams of existing interchange formats, e.g., EDIF, for electronic design and the emerging physical interchange format, PIF.

Several of the SRC research activities have begun to coalesce into design systems. During 1986, the SRC/University of California at Berkeley Center of Excellence began development of an integrated design system for integrated circuits. A new object-oriented data manager and editor, OCT/VEM, which supports design in a distributed computing environment, has been developed as an integral part of the design system (see "Synthesis" research highlight). New macromodule generators and multilevel logic minimization tools have resulted from the effort that used the SPUR chip set at Berkeley as an application target for the new system.

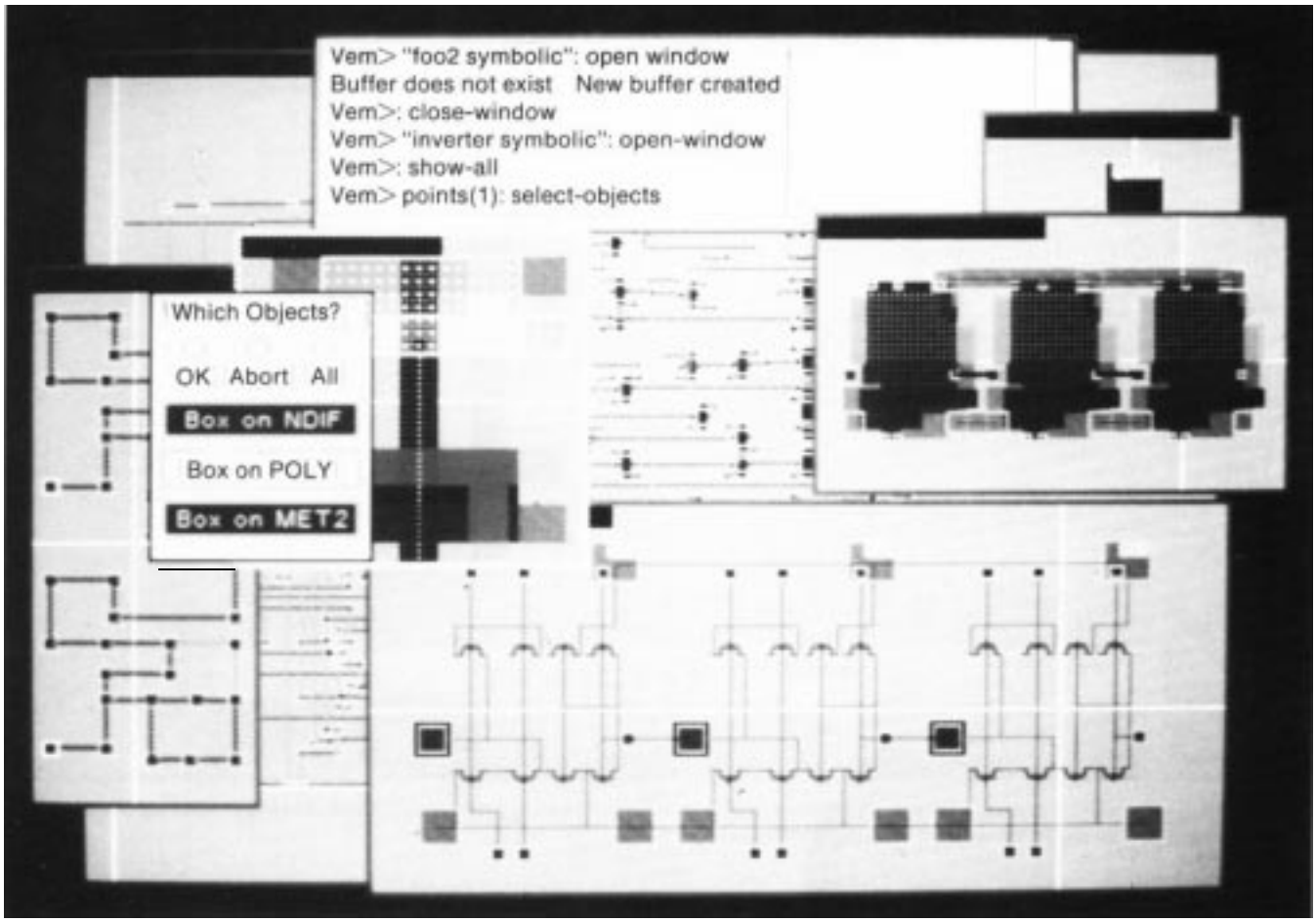
Work continued on the Design Automation System at the SRC/Carnegie-Mellon University Center of Excellence in 1986. A collection of tools has resulted from the research program; and ULYSSES, an expert system design environment, has been developed to aid the IC designer in selecting and linking design tools in the Design Automation System.



A View of the Design Process

Design Systems are not only needed to execute chip-level synthesis and verification but are also needed at the technology levels as well. As an example, the Process Engineer's Workbench that is being developed at Carnegie-Mellon is a design system that is intended to support the design of processes to achieve a specified set of circuit-level performance characteristics in the face of the random disturbances that can occur at each processing step. Another effort that is underway at the SRC/Berkeley Center is to link the SIMPL and SAMPLE tools that model device profiles at arbitrary cross sections and lithography processes, respectively, to other device and process modeling tools such as PISCES and SUPREM at Stanford. The new physical interchange format, PIF, will be used to link these tools to provide an integrated modeling, simulation, and diagnostic system for the process designer.

Graphic contributed by
Pallab Chatterjee,
Texas Instruments Incorporated

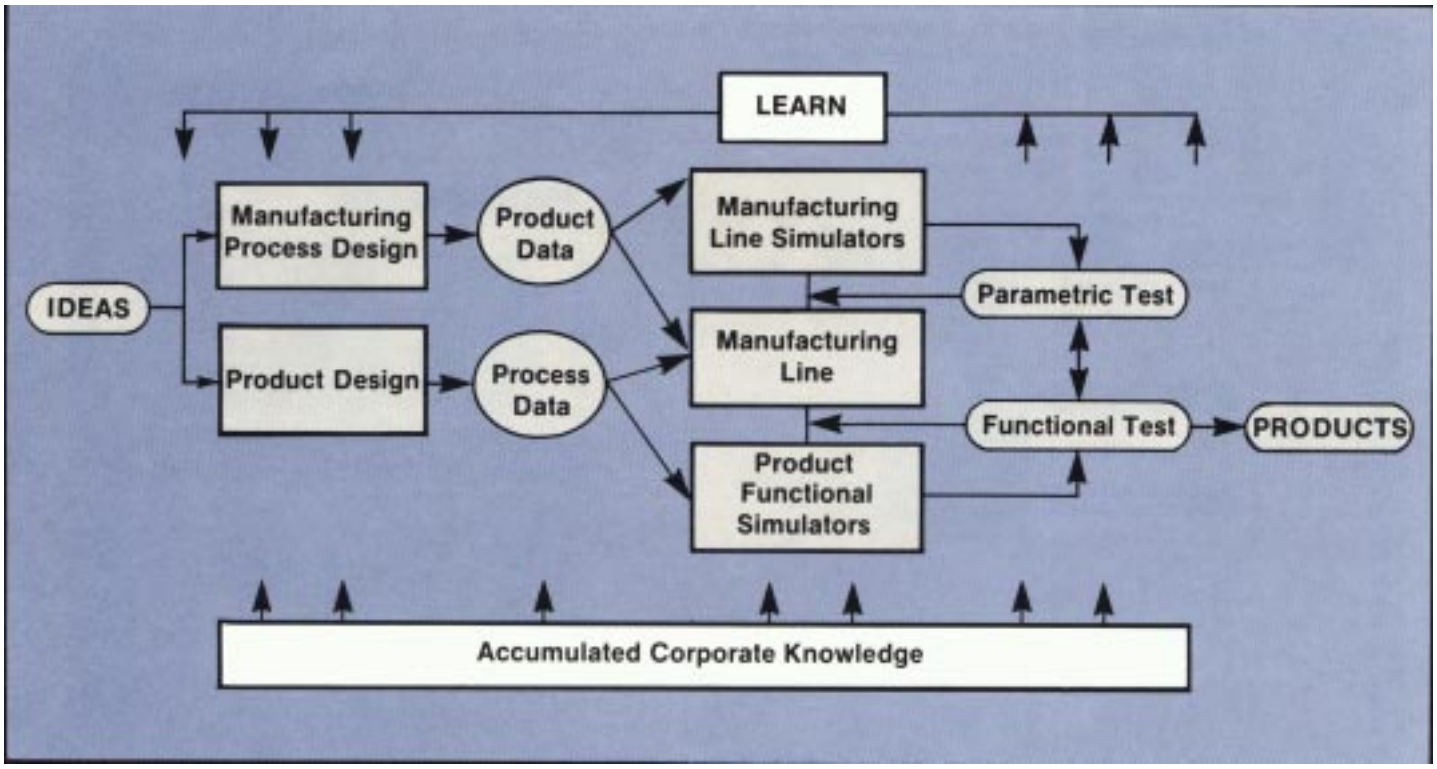


OCT, Object Oriented Data Manager, University of California at Berkeley

Synthesis

Under SRC support, the Berkeley Synthesis Project is a major effort in the area of logic synthesis, module generation, and macrocell placement and routing. The short-term goals are to develop a system with the capability of implementing a microcomputer design, beginning from a combinational logic and latch description and extending to silicon without manual intervention, and to create a layout that is equal to, or better than, a manual design in terms of both area and timing. To date, the focus has been on the development of new synthesis techniques for multilevel combinational logic, embodied in the program MIS; development of a new approach to macrocell placement and routing, implemented in the MOSAICO system; and to integrate these tools in a general-purpose, computer-aided design framework. The framework consists of an object-oriented data manager, OCT, and an associated editor, VEM. In addition, a number of new module generators have been developed for the implementation of both sequential and combinational logic blocks. The researchers are attempting to reimplement SPUR, a VLSI-based multiprocessor under development in the Computer Science Division, as a vehicle for measuring progress. Long-range work on this project includes emphasis on the timing requirements of such chips in both the synthesis and placement/routing phases of design, and as high-quality power and ground routing at the macrocell level. When these "low-level" tools are in place, plans include extension of the existing system to the architectural and behavioral levels of design, using the existing system for testing implementations. Plans also include using the synthesis system for comparison of different design styles and for retargeting designs to the emerging Sea-of-Gates semi-custom approaches.

Professors AR. Newton
A.L. Sangiovanni-Vincentelli,
and C.H. Sequin
University of California at Berkeley



FABLE is a knowledge representation language, specializing in manufacturing processes. FABLE is being created for use as a software tool to automate semiconductor manufacturing.

Manufacturing Automation

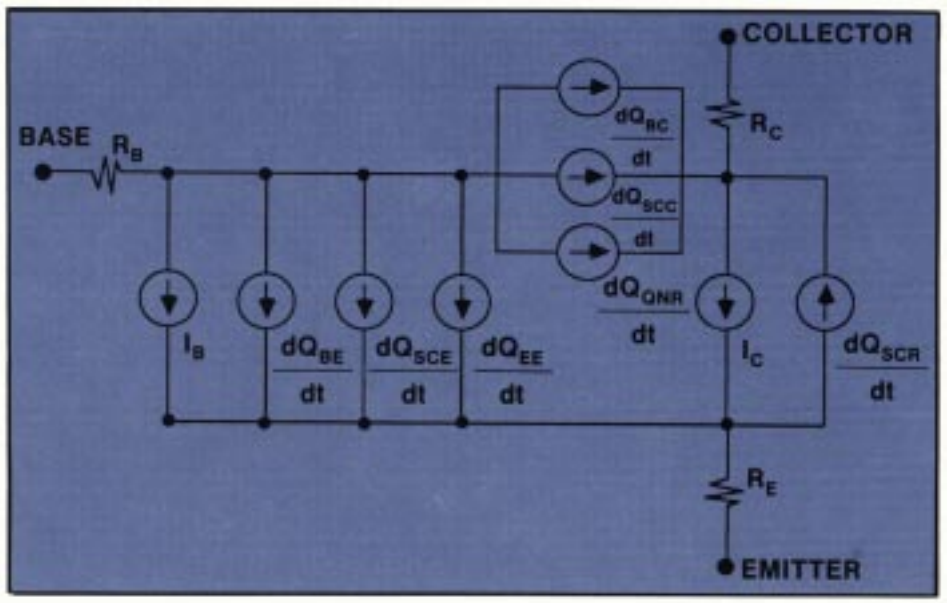
In the Manufacturing Automation project, new high-level programming languages, such as FABLE, are being designed that use several levels of abstraction to obtain the complete specifications for a sequence of semiconductor manufacturing operations. To demonstrate that these specifications are correct, they will be applied to control both automated manufacturing and simulation. This project is developing software technology to maintain and disseminate information about manufacturing operations. Investigators from both the Computer Science and the Electrical Engineering Departments are involved. During the 1986 contract year, a set of hardware and software tools were identified and acquired to support the continued development of FABLE. Four applications projects have been identified that will serve both to determine specific requirements for FABLE and to implement specific parts of FABLE to satisfy these requirements. A course in 'Automation of Semiconductor Manufacturing" has been conducted on campus for the first time; and the research team at Stanford has started a nationwide electronic mailing list, IC-CIM, for discussion of topics in computer-integrated manufacturing of integrated circuits.

Professor Krishna C. Saraswat
Stanford University

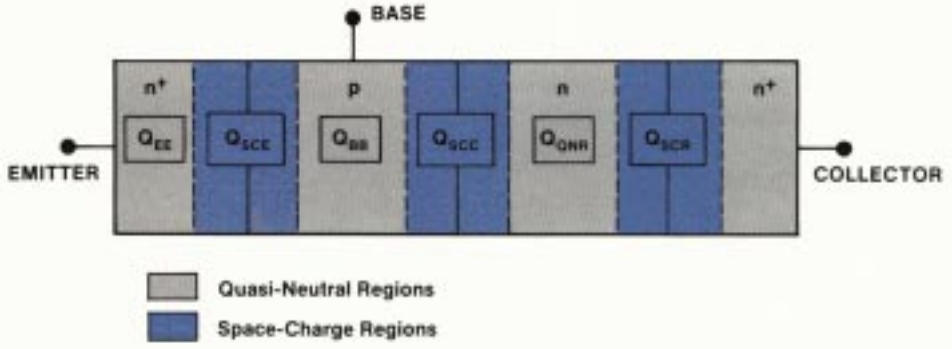
Bipolar Technology

Advanced bipolar technology, producing submicron self-aligned device structures with polysilicon contacts, has created a need for a new bipolar transistor model with more sophistication than existing ones. The SRC has reinitiated research efforts to produce models adequate for this submicron bipolar transistor realm. The new large-signal model, being developed by the University of Florida, is physical and charge-based, in contrast to the earlier empirical, capacitance-based Gummel-Poon (GP) model. The high-current effects (in the base and the epitaxial collector), which become pronounced in contemporary scaled bipolar transistors, are properly accounted for in the new *model. Both ohmic and non-ohmic quasi-saturation* are *modeled by allowing for the formation of a current-induced space-charge region with a moving boundary in the conductivity-modulated epitaxial collector. The transport in the quasi-neutral base is characterized, without resorting to the empirical GP charge-control representation, by extrapolating the analytical solutions for current obtained for low and high injection, and combining the composite solution with the fundamental integral-charge-control relation to describe the charge. The charge-based formalism, in conjunction with proper charge partitioning, readily permits the inclusion of the inherent nonreciprocal transcapacitances which reflect the time delays in the transistor. The new model has been implemented in SPICE2 via user-defined controlled* sources. *When the development is complete, the model will be written into the circuit-simulator code. The implemented model is quasi-static and one-dimensional. Non-quasi-static and multidimensional effects will eventually be incorporated semi-empirically. With the limited empiricism, the model is applicable over a wide range of operating conditions, and it facilitates straightforward parameter extraction without excessive optimization.*

Professor J.G. Fossum
University of Florida



Network Representation of the Charge-Based Bipolar npn Transistor Model (above) with Reference to the Regional Charges in the One-Dimensional Structure (below)



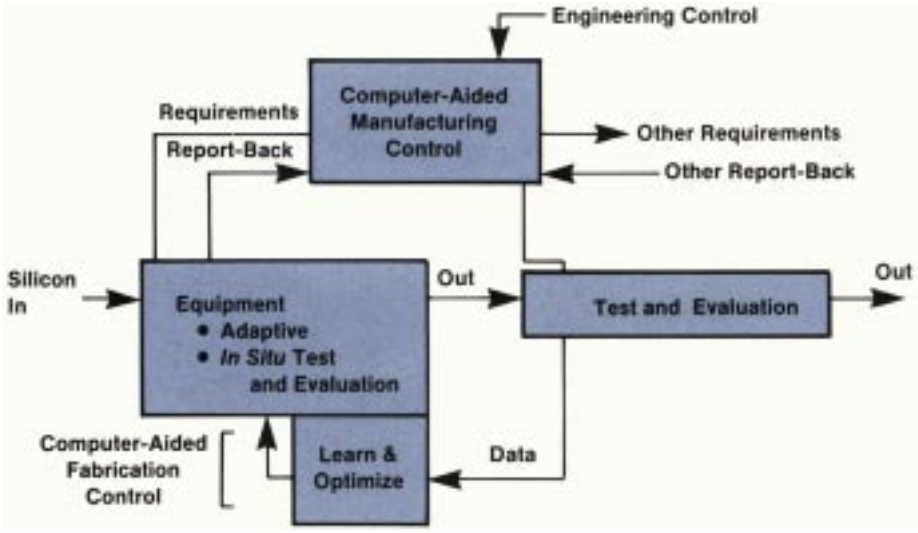
$Q_{B\,B} = Q_{BE} + Q_{BC}$ (charge partitioning)

Factory Automation and Manufacturing

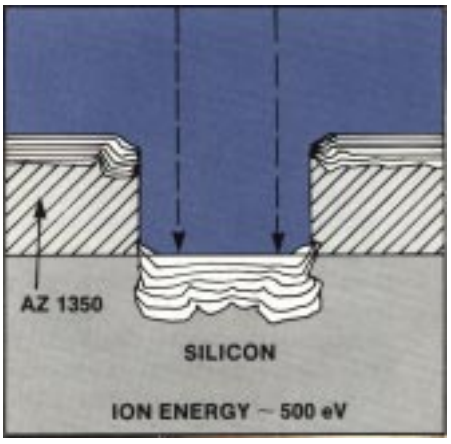
The 1994 integrated circuit factory must demonstrate a three-level hierarchy of control: (1) operation control, (2) process control, and (3) process design. Operational control covers process flow execution and inventory control. Unit processes and their control must assure that the equipment yield the anticipated results at the expected particulate contamination level. The illustration below shows how future generations of processing equipment will function. The inclusion of adaptive control will be a result of fully-functional computer-integrated manufacturing (CIM) and computer-aided fabrication (CAF). Process design covers the monitoring and feedback functions to assure that the process parameter targets are met and that process-induced defects are kept in control. Inherent in the objective of the SRC Manufacturing Sciences program is the development of scientific and engineering talent that can contribute to this field of knowledge and skills that can be applied in the semiconductor manufacturing industry.

In any fabrication fine, two forms of process control are possible: quantity control and quality control. The aim of quantity controlis to maximize throughput in a given period of time, while the aim of the quality control system is to maximize the number of acceptable chips by maximizing the production yield. By developing a realistic profit function and formulating an equation for profit maximization, both types of process control can be simultaneously performed.

Requirements for ultra-large-scale integrated (VLSI) products are not consistent with a slow learning curve. International competition will increase in intensity. The United States must have and implement a strategy leading to growth and profitability, even though domestic industry may have to concede continuing advantages to foreign competitors in the cost of labor and the cost of capital.



Functionality of Future Generations of CIM/CAF Ultra-Large-Scale Integrated Processing Equipment



RIE Process Modeling

Automated Reactive Ion Et

The SRC/University of Michigan Program in Automated Semiconductor Manufacturing is using reactive ion etching (RIE) as a process vehicle for examining key issues associated with automated sensing, control, and facilities integration. A dual-chamber SEMI-1000 RIE is now installed and is being interfaced with a 10Mbs MAP network in Michigan's new Solid-State Fabrication Facility. This network will be used in a prototype testbed for process automation, offering a guaranteed response time, message prioritization, and a hierarchical facility architecture. Software

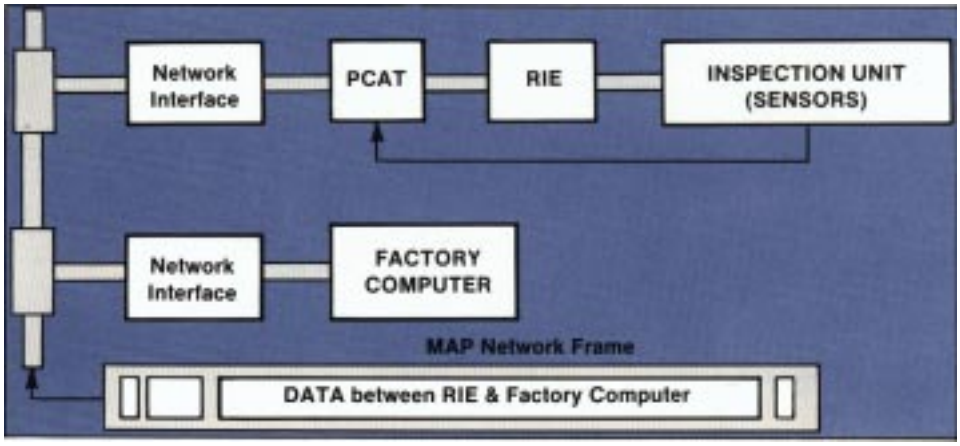


Photo and Diagram Above: New Solid-State Fabrication Facility, University of Michigan

hing

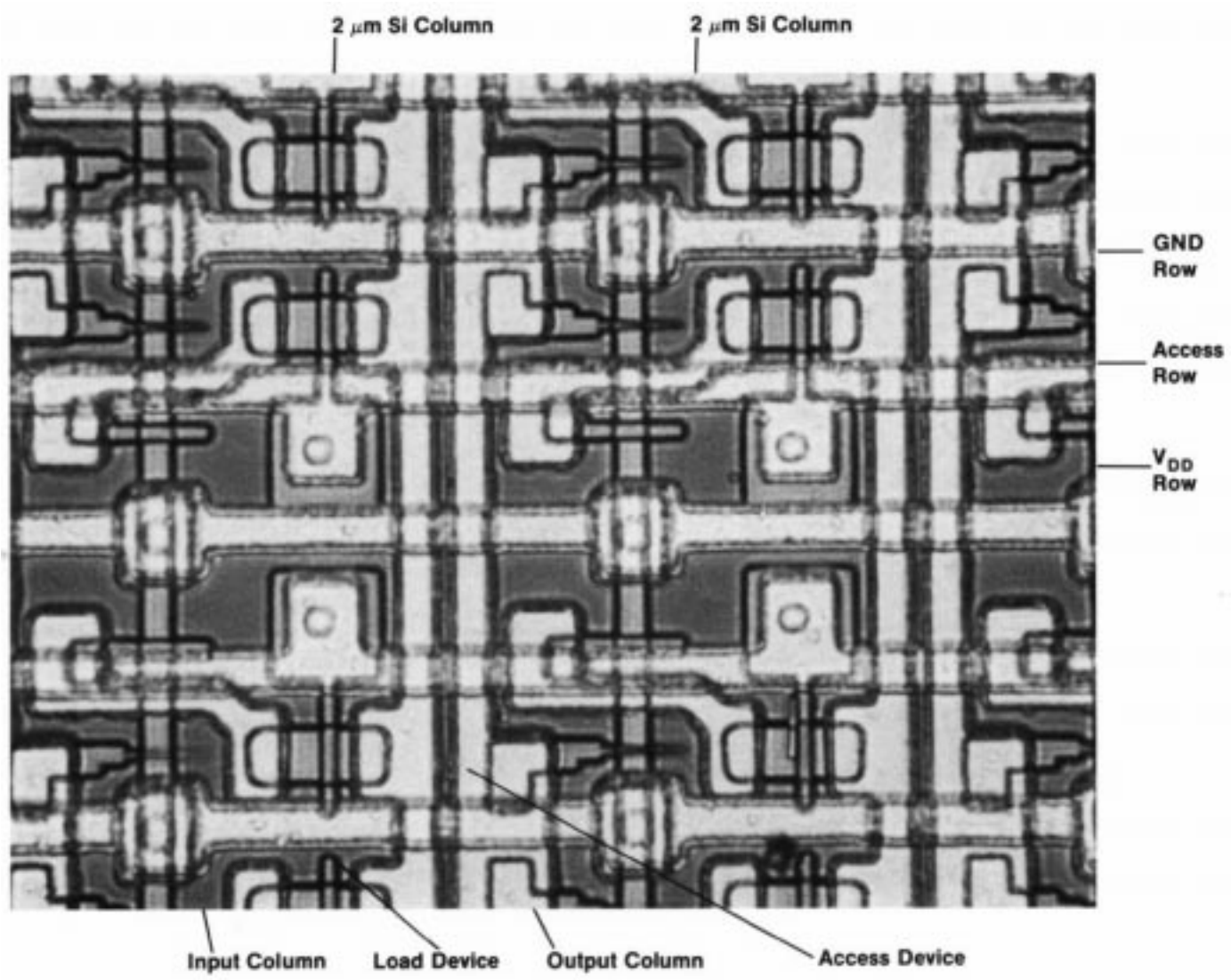
drivers for this network have now been developed as well as a network interface for the SECS protocol. Companion work in advanced RIE process modeling now allows the calculation of two-dimensional microstructure etch topographies for a variety of etching parameters. These models will facilitate the automatic fine-tuning of etch characteristics and process interpretation via an RIE expert system, also under development. Work on monolithic integrated sensors for pressure, gas flow, and gas analysis will provide additional data for equipment control.

Professor Ken D. Wise
University of Michigan

Computer-Integrated Manufacturing (CIM)

Efficient operation of an IC production process requires the timely acquisition, processing and utilization of data at many levels. At the equipment level, accurate models of the equipment are needed, and advanced sensing techniques are required in order to effectively achieve real-time control of the equipment-level component of the manufacturing process. At the operational level, data are required on such attributes as the status of work in progress, manufacturing schedules, equipment outages and maintenance schedules, and process yields. Ideally, expertise on the operation of individual equipment and on sets of equipment should be provided by the information system to the operations personnel. The chip designer must also be information-linked to the manufacturing information system, since a know/edge of yield and performance-loss mechanisms due to anomalies on the manufacturing line can sometimes be ameliorated by modification of design styles and/or design rules. In addition, test patterns generated at the design level must be linked to the test application equipment on the manufacturing floor. The implication of the requirement for ready access to many kinds of data by many different end users in order to achieve an overall efficiency in operation has motivated the conduct of SRC research on Computer-Integrated Manufacturing. CIM is characterized by research to define information system architectures, data management methods, and communication requirements andprotocols; by the application of Knowledge-Based Engineering Principles; and by the development of improved dynamic scheduling algorithms.

One-Quarter Micron NMOS Inverter Array



Device/Circuit Technology

The illustration shows the complexity of a 0.25 micron NMOS inverter array recently fabricated at Cornell University. The enhancement mode switch device has a physicalgate length of 0.25 μm and a gate width of 2 μm. A pair of flipped inverters are *located between horizontally running V_{DD} (top), GND (middle), and* a *flipped V_{DD} (bottom) lines laid out in global metal (Al). An access transistor connects the output node of each inverter to vertical column lines running in local metal (TiW/Al). The inverter inputs are connected to column input lines also running in local metal next to each output column. The gates of the access transistors are controlled via local metal row lines running between each V_{DD}-GND line pair. The scale marker shows the 2 μm width of the active region of the 0.25 μm NMOS switch device running vertically between the column lines. Since this chip has been fabricated using hybrid, direct-write electron beam lithography for gates, and optical lithography for all other features, only the active devices have been scaled to 0.25 μm size. Especially, local-metal to global-metal contacts are disproportionately large. A full electron beam lithography basedprocess is currently being developed.*

Professor J. P. Krusius
Cornell University

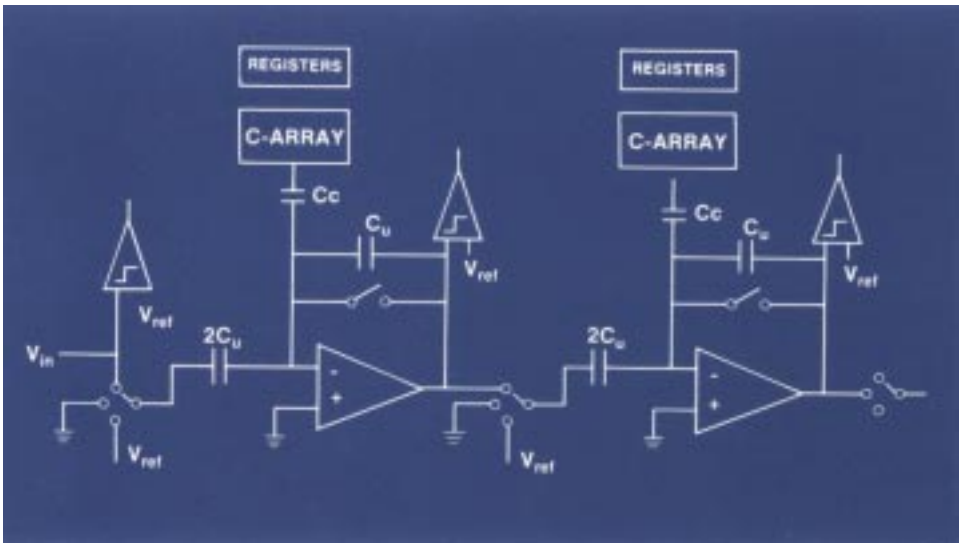
Linear Integrated Circuits

Digital signal processing is widely expected to assume a crucial role in sustaining the growth of semiconductor electronics. However, the scaling of MOS VLSI technology that makes digital processing increasingly attractive also severely constrains the dynamic range available for implementing the interfaces between the analog and digital representation of signals within that same technology. Oversampled data conversion architectures offer a means of resolving this dilemma. In these architectures, sampling at well above the Nyquistrate is combined with negative feedback and digital filtering to efficiently exchange resolution in time for that in amplitude. Such converters thus exploit the enhanced density and speed of scaled digital circuits to ease the difficulty of integrating complex analog circuit functions. An SRC-sponsored research program has been initiated at Stanford under the direction of Professor Bruce Wooley to explore in depth the design of oversampled data acquisition systems within the context of their implementation in a CMOS VLSI technology.

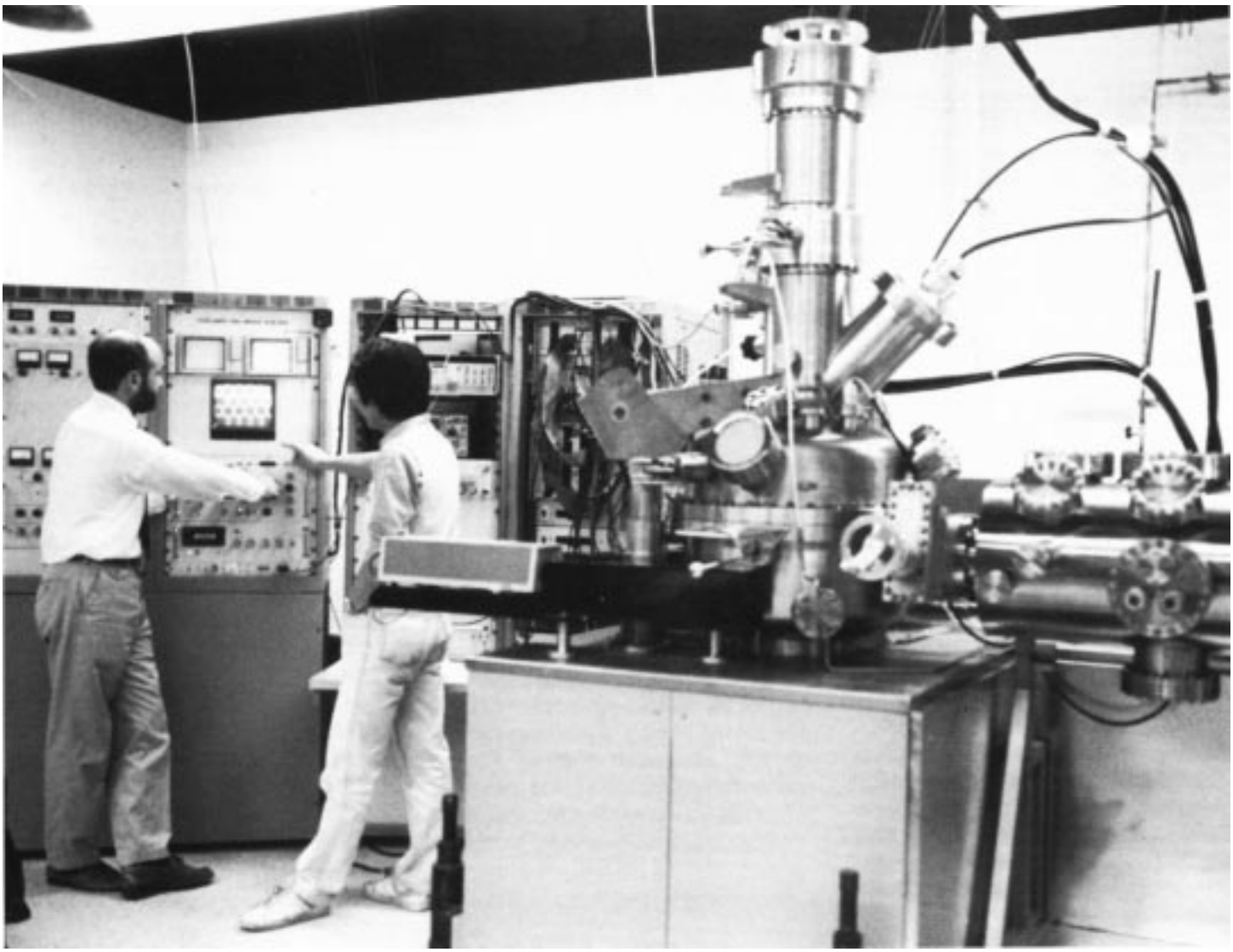
A second project to design data converters for digital signal processing applications is underway at the Massachusetts Institute of Technology. This converter will use the new BiCMOS process being developed at MIT in order to achieve high performance and accuracy. A self-calibrated pipeline A/D converter architecture, as shown in the accompanying figure, is planned as the test vehicle for the new BiCMOS process. The architecture shown offers reduced complexity over other pipelined schemes because sample and hold elements have been eliminated and an analog multiplier is not required. The immediate design goal of this project is to develop a 16-bit 500 KHz converter using a standard three micron CMOS process. The performance characteristics of the CMOS Op Amp and comparator that have been designed are listed in the following Table.

3 μ CMOS Op Amp Performance	
Gain	$5x10^6$
Unity Gain Bandwidth	10 MHz
Capacitive Loading	10 pF
Slew Rate	0.3 V/ns
Power Dissipation	47 mW
CMOS Comparator Performance	
Delay	60 ns
Power	10 mW

Several other projects are underway to improve the quality of design support available for linear integrated circuit designers. At Georgia Tech, an analog design platform, called AIDE2, has been developed to explore design methodologies for switched capacitor circuits and mixed analog digital application-specific integrated circuits. Analog design tools must work in the 'assistant mode' for complex designs that push the limits ofprecision andperformance and in the 'compiler mode' for simple designs requiring a unique grouping or interconnection of ordinary analog functions. A second project to develop design techniques for switched capacitor signal processing circuits, which take advantage of scaled technologies and that close/y approach the fundamental limits in area and power, is underway at the University of California at Berkeley. Researchers at Carnegie-Mellon University are investigating the application of Knowledge-Based Engineering principles to the design of a broad class of operational amplifiers and, ultimately, data converters. A functional analog circuit designer's workbench that supports incremental simulation of complex analog circuits has resulted from a research activity at the California Institute of Technology. A research activity at Nebraska is developing design principles for the synthesis of balanced, continuous-time, high-performance analog circuits in MOS technology.



Pipelined Self-Calibrating A/D Converter Showing the First Two Stages



Focused Ion Beam System

A major SRC-sponsored program in the area of focused-ion beam (FIB) technology is underway at Rensselaer Polytechnic Institute. This research effort has the overall objective of developing FIB technology for the fabrication of novel semiconductor devices. The three major research tasks of the overall program are FIB system development, liquid metal ion source research, and novel devices.

The FIB system shown in the accompanying photograph was installed at RPI in March, 1986, and logged approximately 500 hours of "beam" time during its first 12 months of operation. The sample insertion and preparation chamber is located on the right; the ion column and the working chamber are located in the center; *and two high-voltage and source-control units, and the detection and display rack are located on the left. ion sources used in the system have been Ga, Au/Si, Pd/B. Ion beam diameter as small as 1500-2000 angstroms has been observed at an accelerating energy of 95 Kev.*

Professor A.J. Sfeckl
Rensselaer Polyfechnic Institute

Focused-Ion Beam System at Rensselaer Polytechnic Institute. Professor A.J. Steckl and graduate student Cheng-Ming Lin are shown observing a focused-ion beam image of a calibration grid.

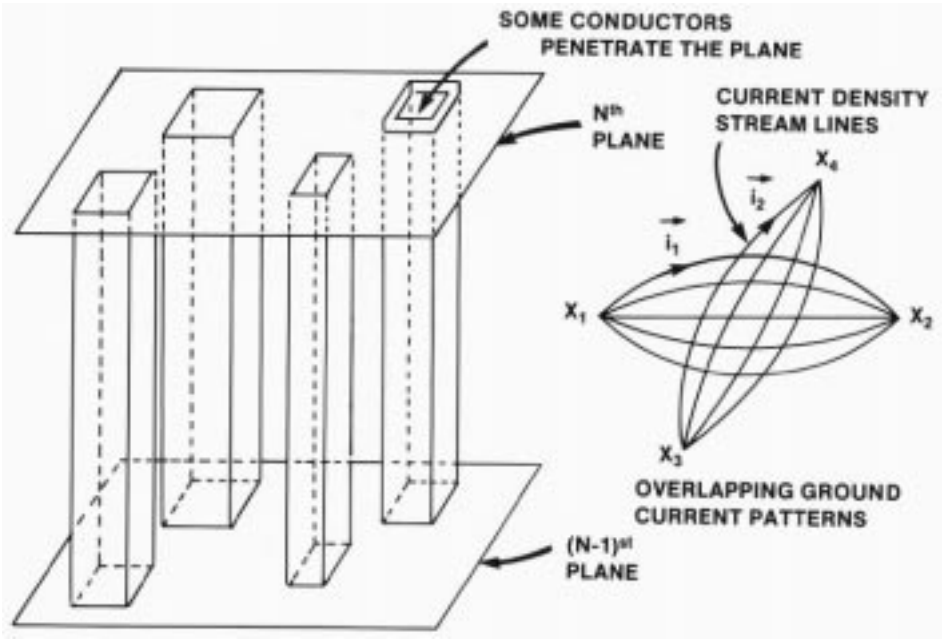
Technology Transfer from the University of Arizona

Two software packages with documentation, developed by SRC researchers at Arizona, were requested by and delivered to several member companies in 1986. The companies performed beta testing to prove out the software, and to assess its accuracy and convenience of use.

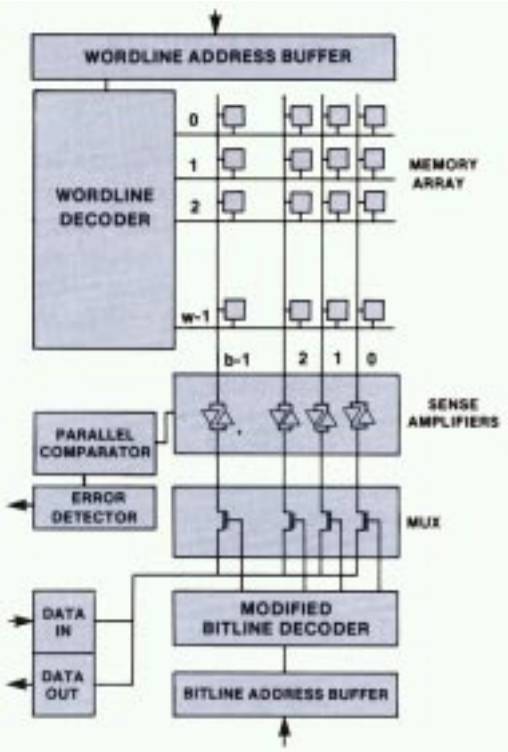
Software called UAC was developed for calculating the Maxwellcapacitance matrix for 2-D systems of conductors of arbitrary cross section, and of arbitrary number, placed in arbitrary positions in one of three possible dielectric/ground plane geometries. UAC also calculates the associated inductance matrix for the conductor systems. UAC enables the calculation of conductor fine capacitance, and in certain cases inductance, for two-dimensional fine-to-ground and fine-to-fine geometries. Characteristic impedance, and coupling impedance, can be calculated from the output. Companies serving as beta test sites for this software include AT&T Bell Laboratories, Burroughs, Du Pont, GTE, Honeywell (three beta test sites), General Motors/Hughes Aircraft, IBM, Motorola, and Rockwell International.

A second design/analysis software package, called PCUAL, enables calculation of line inductance directly, including cases where calculation of the Maxwell capacitance matrix may be difficult. Companies serving as beta test sites for this software include AT&T Bell Laboratories, Burroughs, Du Pont, Hewlett-Packard, General Motors/ Hughes Aircraft, IBM (two beta test sites), Motorola, and Rockwell International. Each company agreed to apply UAC1.1 to problems of the company's choice and to share (with the University of Arizona) qualitative and quantitative results of that application. While comparing UAC1.1 with more cumbersome but well-proven analysis tools, one member company employee has written, "I am pleased to report that our preliminary results indicate that UAC1.1 is quicker, much easier to use, and very accurate over our range of application."

Professor J.L. Prince
University of Arizona



Configuration Used for Inductance Modeling



RAM Organization Designed for Testability

Figure illustration for "Testable RAM Design" By P. Mazumder and J.H. Patel, Computer Systems Group.

Testable RAM Design

Conventional testing strategies for random access memories (RAMs) usually require a number of test patterns for an n-bit memory element that is proportional to n^2. The implication is that RAM test time, and hence cost, becomes prohibitive as memory sizes continue to increase. Researchers from the SRC Program in Reliable VLSI Architectures have recently proposed a testable RAM design that may drastically reduce RAM test time. This design incorporates a modified bit-line decoder and a parallel comparator so that in test mode several hundred bits are accessed and compared in one cycle. The scheme is quite general and can be used to implement various pattern-sensitive test algorithms for RAMs and content-addressable memories, and is also amenable to built-in self-test implementation.

Professor J.H. Patel
University of Illinois at Urbana/Champaign

Metrology and Sensors

Particle transport to a wafer surface and capture by that surface depend on many variables such as aerosol velocity and particle size. While gravity is a minor mechanism for submicron aerosol capture by a wafer, it can be the dominant mechanism for capture of larger aerosol particles. Diffusion, interception, and inertial impaction are the classical mechanisms by which filters capture submicron particles; they apply to wafers as well. All the aerosol properties that influence these mechanisms will affect particle deposition on a wafer. In addition, the wafer surface itself may be a significant variable primarily through electrical capture forces. Electrical charges on a surface create electricalcapture forces that can make up an important mechanism for the deposition of submicron aerosol particles on that surface.

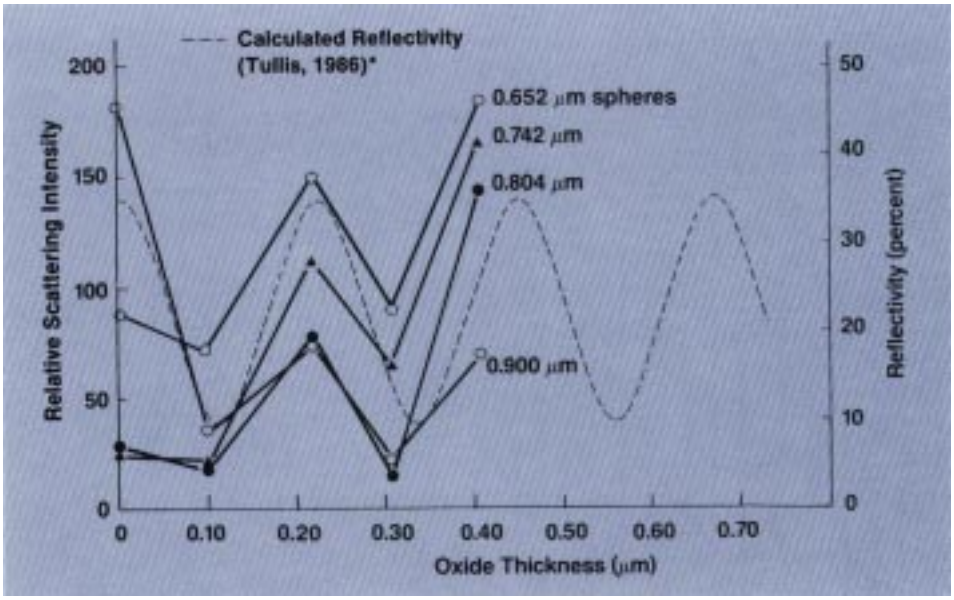
Electrostatic forces will receive special emphasis in upcoming studies of particle transport at Research Triangle Institute. The use of patterned, electrically biased silicon substrates to deliberately create local areas of potentially enhanced electrical capture is proposed as part of the test matrix. The dependence ofparticle deposition upon electrical forces will thus be studied with higher spatial resolution than heretofore possible. Appropriate test structures include both metallized patterns on oxides and oxidized silicon surfaces.

Subsurface imaging methods are important for evaluation of device geometries which are inherently three-dimensional. Accurate depth profiling methods are necessary for failure analysis and process evaluation. SRC research at the University of North Carolina at Chapel Hill has shown that the electron-beam-induced current (ERIC), BSE, and Time-Resolved Capacitive Coupling Voltage Contrast (TRCCVC) imaging modes provide information about buried structures and layer thickness.

Particulate Research: The Role of Particles in Yield Considerations

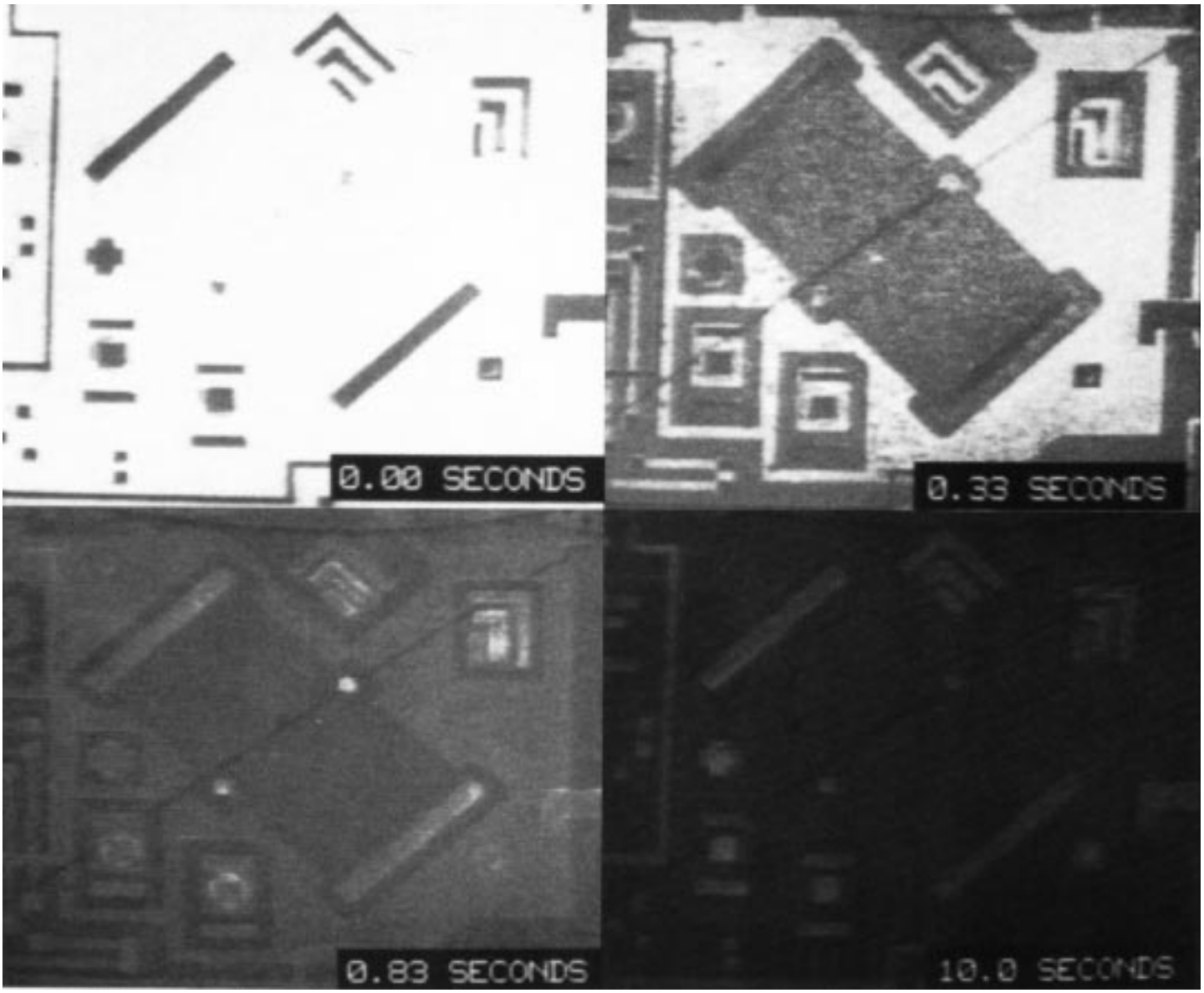
To be competitive, semiconductor manufacturing processes must achieve high yields. Since particulate contamination is one of the major yield detractors, the ability to control and reduce particulates on wafers is crucial to success. This project has focused on two important aspects of the overall problem: the measurement of small particles on silicon wafer surfaces, and the influence of wafers. One of the most significant accomplishments of this year's work was the documentation of the non-monotonic relationship between particle size and scattered light intensity in laser surface scanning tools. Over the past five years, laser scanners have become routine tools used to measure particulate contamination on production silicon wafers. They detect and size single particles resting on an unpatterned wafer by measuring the intensity of light scattered through a known scattering angle or angles. However, the intensity of the light scattered by a surface particle depends not only on its size but also its shape, index of refraction, and the reflectivity of the wafer surface. This last dependence means that the relative scattering intensity of a given surface particle varies with the oxide thickness of the silicon wafer. For example, as shown in SRC-sponsored research at the Microelectronics Center of North Carolina, the relative scattering intensity of submicron polystyrene latex spheres (a transparent particle) deposited on silicon wafers of varying oxide thicknesses varies in phase with the calculated surface reflectivity. Also noteworthy is the observation that, over a narrow size range in which the particle size is similar to that of the laser wavelength, smaller particles can scatter more light than larger particles. While complete theoretical solutions to the problem of light scattering by a transparent particle resting on a reflecting plane do not yet exist, these data make clear the need for careful calibration of a laser scanner in order to correctly interpret light scattering from surface particles.

Dr. R.P. Donovan
MCNC/Research Triangle Institute



The effect of water surface reflectivity upon surface particle light scattering. (Spheres are transparent polystyrene latex)

*Tullis, B.J., "Measuring and Specifying Contamination by Process Equipment," Microcontamination, 4 (1), pp. 51-55, 1986.

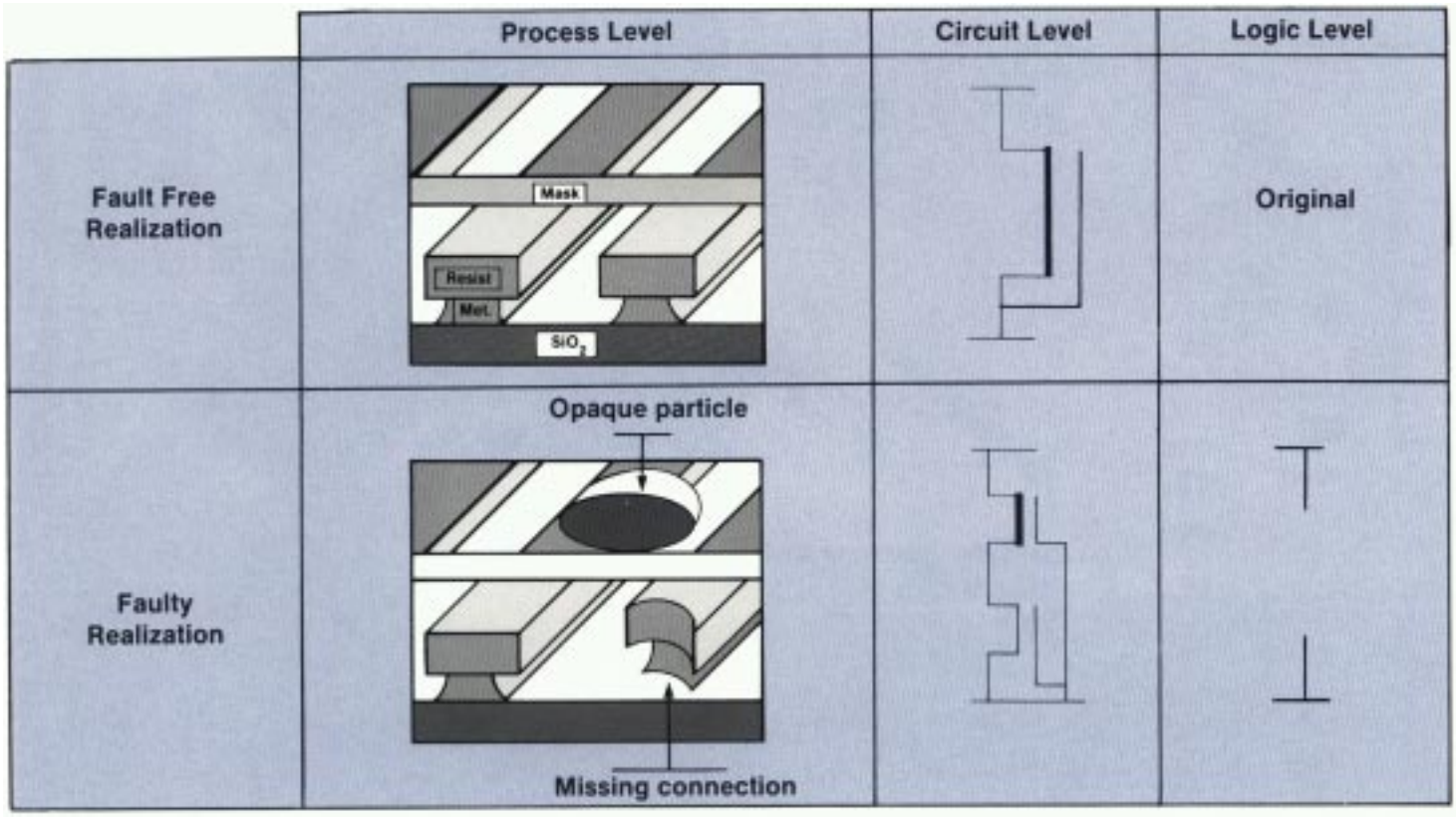


CCVC images of a floating Hall effect device at different times after initial electron beam exposure. The contrast is generated by the depth dependent response of low energy scattered electrons.

Analysis of Microelectronic Devices Using Scanning Electron Microscopy

At submicron dimensions, mechanical probing of devices is nearly impossible and usually destructive when applied to integrated circuit fabrication technology. The electron beam of the scanning electron microscope (SEM) is an alternative to mechanicalprobes and is a standard tool in the microelectronics industry. Unfortunately, many of the SEM imaging modes can potentially induce damage in radiation-sensitive devices. Low energy (<1 keV), nondestructive SEM imaging techniques that avoid radiation damage are being developed and modeled in this SRC project. Capacitive coupling voltage contrast (CCVC) is a low-energy method that provides both voltage and depth informa lion of structures buried under passivation. CCVC utilizes the dynamic response of low energy electrons near the surface to changes in voltage or differences in structure depth. Voltage resolutions of 40 mV have been recorded using this technique, with a spatial resolution of less than one micrometer. Depth profiling has been performed on both biased and floating devices. Analysis can be performed during manufacturing, since no bias is required and no mechanical probing is needed.

Professor R.H. Propst
University of North Carolina at Chapel Hill



Inductive Fault Analysis: Abstraction Levels

Inductive Fault Analysis

For Very Large Scale Integrated Circuits, exhaustive testing to insure proper functional performance is often prohibitively expensive. In order to reduce this cost, faults should be "graded" so that those most likely to occur are tested for first. Towards this end, the concept of Inductive Fault Analysis (IFA) has been developed. IFA proceeds by determining the set of defects most likely to occur in the manufacturing process and then determining the effects of these defects on functional performance. This information is then used to guide test vector generation. The inductive Fault Analysis procedure consists of four major steps..

1. *Generation andplacement of physical defects employing statistical data obtained from the fabrication process;*
2. *Extraction of geometric and structural faults caused by those defects;*
3. *Abstraction of those faults to the circuit and logic levels of behavior;*
4. *Classification of fault types and the ranking of faults based on the likelihood of their occurrence.*

Given the layout of an integrated circuit, an accurate customized fault model and associated ranked fault list can be generated automatically by IFA to take into account technology, process, and layout characteristics. While this approach is still new, it has shown some surprising results. For example, an investigation of one CMOS circuit yielded the following observations:

1. *Only about two-thirds of the faults could be characterized with the traditional single and multiple line stuck-at (zero or one) model;*
2. *Fewer than five percent of the faults involved transistors stuck at open;*
3. *Approximately one-third of the faults were bridging faults;*
4. *Unusual faults, such as the creation of new transistors, were possible.*

The fault lists generated via the inductive fault analysis method are used as input to a prototype switch-/eve/ test pattern generation and evaluation system consisting of three major components:

CG — Cube genera lion program;
TG — Test generation program, employing search and back&acing; and
MMS — An interface to the fault simulator, MOSFLS.

Work is underway to extend the prototype system to handle test generation for generalized bridging and break faults, integrated logical and topological testing, and the generation of multipattern test sequences immune to delays and hazards.

Professor John P. Shen
Carnegie-Mellon University

Interconnect

The understanding of the metallurgy of thin films is key to the use of silicides in the fabrication of integrated circuits. In particular, the stability of silicides on polycrystalline silicon is important because of the application of this structure to interconnections on CMOS gates. During investigations by a research team in the Department of Materials Science and Engineering at Cornell, it has been discovered that the polysilicon layer can be consumed, allowing direct contact between silicide and gate oxide as well as deformation of the silicide layer. At temperatures between 850°C and 900°C, depending on the silicide, the fine-grain polysilicon dissolves in the silicide and recrystallizes in large grains of 0.1 to 1.0 micrometers. This solid phase transport and recrystallization is sensitive to the amount of impurities in the silicide or polysilicon. Edge effects can dominate in fine-line structures.

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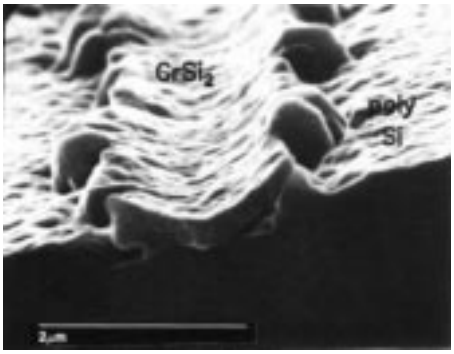
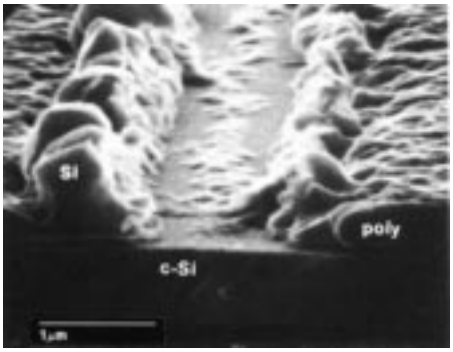
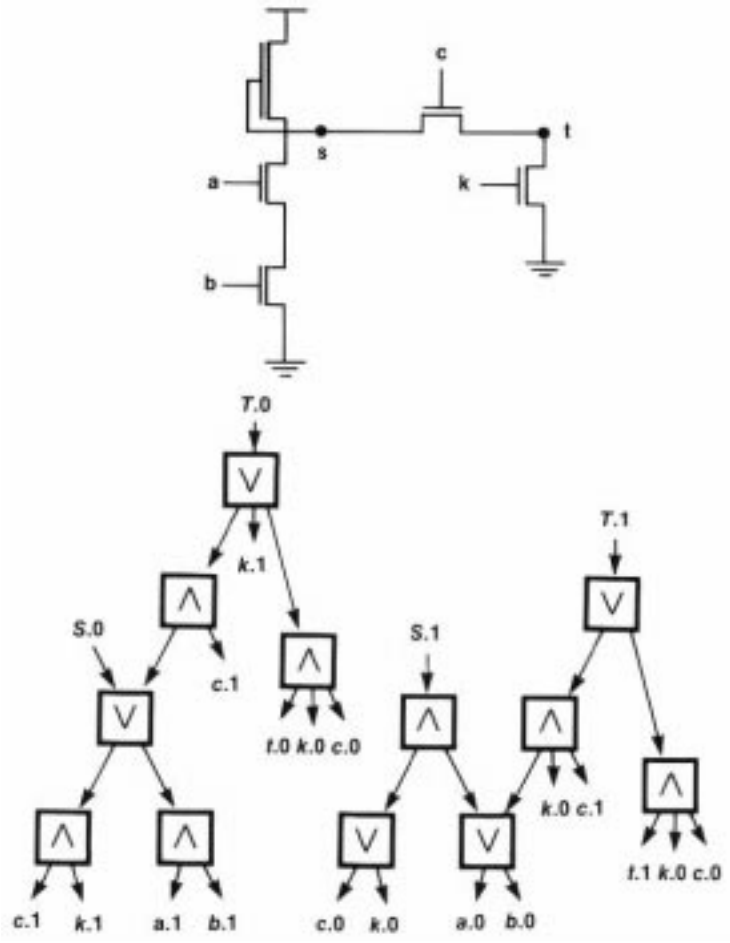
Cornell University



A side view of a $CrSi_2$ layer on poly Si annealed at 900°C showing the deformation of the silicide and the formation of islands.



Removal of the silicide layer shows that the poly Si layer has been consumed by transport through the silicide layer and subsequent recrystallization along the periphery of the silicide lines.



An Example nMOS Circuit and its Boolean Representation. Pairs of variables denote the encoded initial states of the input and state nodes. Formulas *S*1, *S*.0, *T*.1, and *T*.0 denote the encoded new states of nodes s and t.

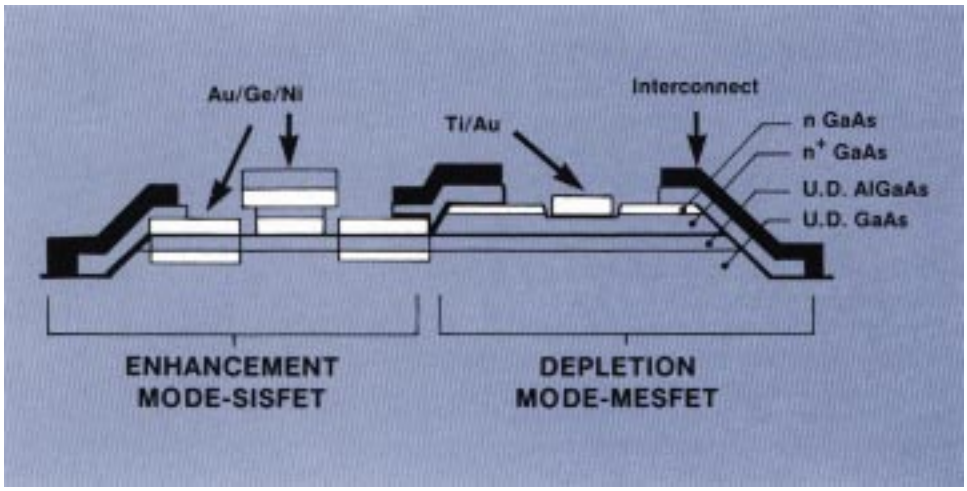
COSMOS

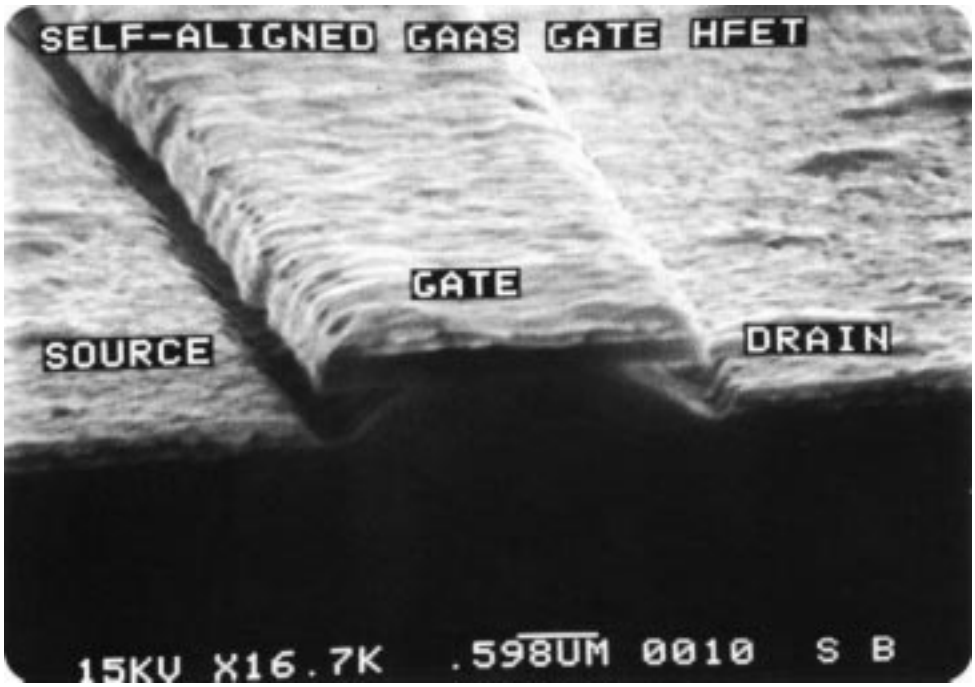
One of the activities in multilevel simulation that has made recent progress is the COSMOS (Compiled Simulator for MOS circuits) project. This project has developed a new method for switch-level simulation, a form of logic simulation that represents a MOS transistsor circuit as a network of discrete switches. This new method yields high performance on conventional computers and promises an efficient mapping onto a variety of simulation accelerators. A preprocessor transforms the transistor circuit into a functionally equivalent Boolean representation. This representation, produced by the symbolic analyzer ANAMOS, captures such aspects of MOS circuits as bidirectional transistors, stored charge, and different signal strengths, By encoding logic values 0, 1, and X with pairs of Boolean variables, it can also capture the effect of indeterminate logic values. For most MOS circuits, ANAMOS can exploit their sparse structure to create Boolean representations of size proportional to the circuit size. For simulation on a conventional computer, the LGCC program transforms the Boolean representation into a set of C language procedures representing the partitioned circuit functions, along with a set of initialized data structures representing the network structure. This code is compiled together with code implementing the event scheduler and user interface to yield a high performance simulation program. The resulting simulator operates an order of magnitude faster than such switch-level simulators as MOSSIM II. Current research includes implementing fault simulation and mapping the Boolean representation onto simulation accelerators.

Professor R.E. Bryant
Carnegie-Mellon University

New Device Concepts

Promising new device concepts are being explored that have the potential to provide improved performance beyond those which can be projected for achievement by 0.25 micron CMOS technology. Many of these concepts are based on quantum domain structures and utilize the flexibility offered by GaAs materials. Additionally, the SRC and the Institute for Theoretical Physics will be co-sponsoring a workshop to explore the transport properties of device structures in the realm of mesoscale physics. These investigations could lead to the basis for computers that perform with new architectural concepts which are not based on the use of binary elements.

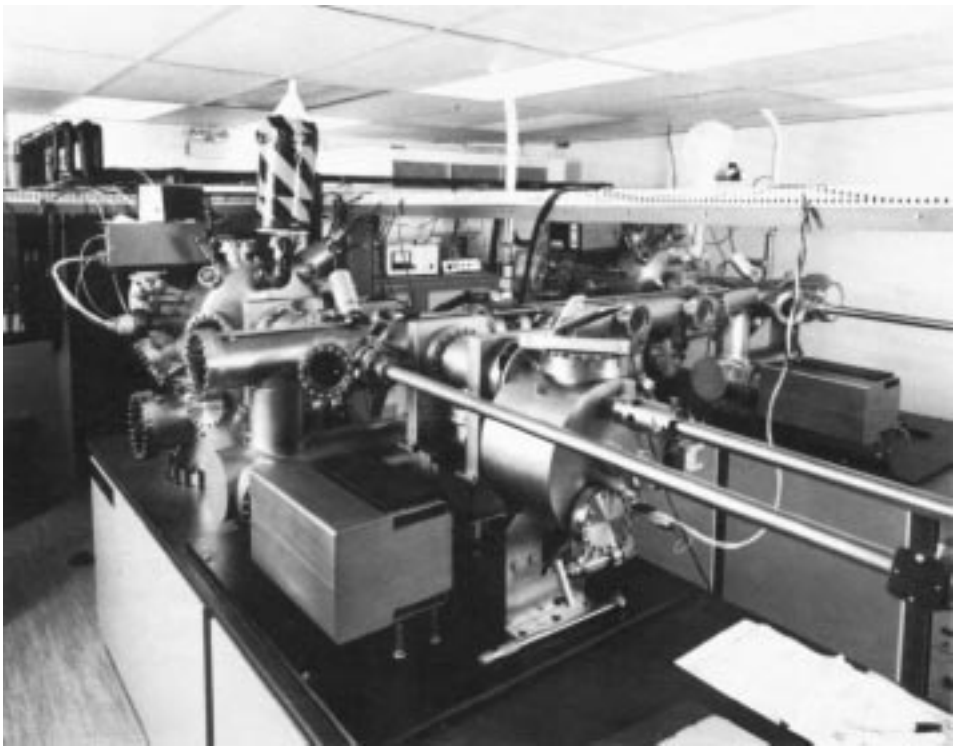




GaAs-Gate Field Effect Transistor Devices

Recently, the joint SRC team of researchers from the University of California at Santa Barbara and Stanford University has developed III-V devices that incorporate a semiconductor-insulator-semiconductor (SISFET) type structure which is interesting because of its potentially controllable and highly uniform threshold voltages. The threshold voltages of such devices are independent of the doping and thicknesses of the epitaxial layers, making SISFETs a prime candidate for use in future LSI or VLSI III-V circuits. The incorporation of a SISFET, which operates in the enhancement mode, and depletion-mode MESFET has been successfully demonstrated and is shown schematically in the upper figure. A scanning electron micrograph (SEM), showing the novel self-aligned ohmic metallization used, is shown in the lower figure.

Professor James *L. Merz*
University of California at Santa Barbara



Dual Growth Chamber MBE System, Stanford University

Complementary Heterojunction FET Circuit

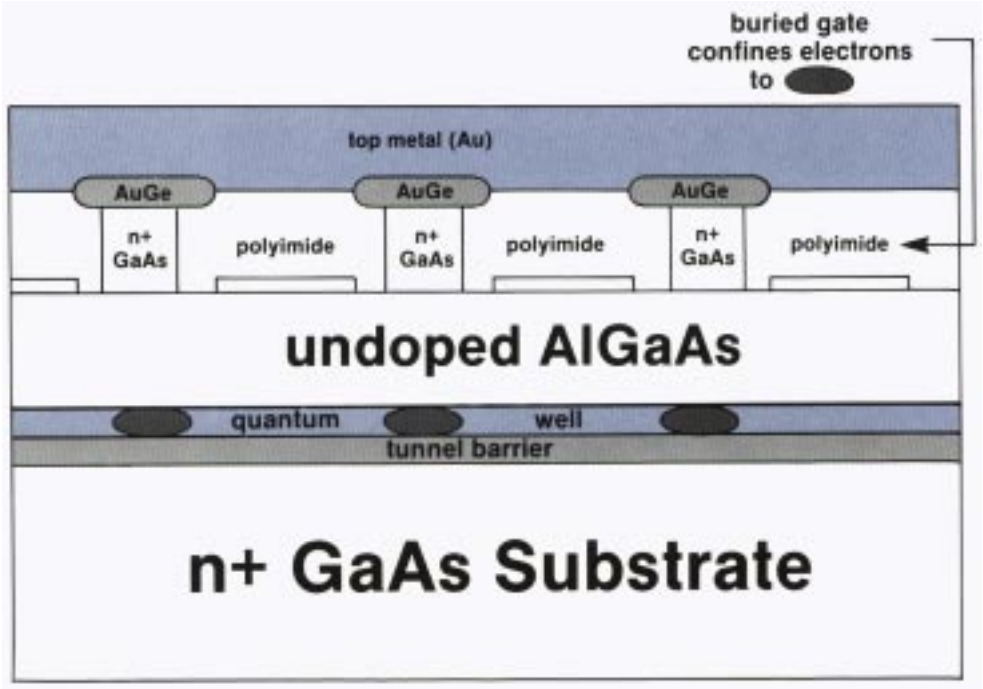
For the tandem growth chamber equipment at Stanford University, molecular beam epitaxy (MBE) is being used in the fabrication of the complex heterojunction device structures that support the research of the Gallium Arsenide Program at the University of California at Santa Barbara. One of the limitations of MBE has been the inability to alternate semiconductor patterning and epitaxial growth. This limitation has been partially due to the backside indium substrate bonding previously used in MBE growth and partially to poor epitaxial growth in small masked windows. During 1986 both of these limitations were overcome by using the dual growth chamber MBE system shown in the photograph.

Professors James S. Harris and
Robert W. Dutton
Stanford University

Quantum Dot Device Structures

At Cornell University, SRC researchers are investigating device structures in which electrons are confined to regions, "quantum dots," of such dimensions that quantization in all three spatial dimensions is important to the properties of the device. The structure chosen for investigation is a two-dimensional electron gas in a quantum well in GaAs/AlGaAs in which lateral confinement is achieved by application of suitable potential to each of a pair of spatially modulated gates above the quantum well (see figure). One gate is a buried Schottky gate in a square mesh configuration with an 8000-angstrom pitch, the other an n+ gate in the holes of the mesh. Tunneling is capacitively induced through an AlGaAs barrier to an n+ substrate beneath the quantum well. Initial characterization has shown strong evidence for isolation of the electron in the quantum well into localized regions under the n+ gate as desired.

Professor Noel C. MacDonald
Cornell University



GaAs/AlGaAs Quantum Well Two-Dimensional Electron Gas Structure

Challenges

The SRC is the organization through which most of the U.S. semiconductor industry, now with government participation, seeks to identify and can-y out generic research addressing national needs in semiconductor technology. Two primary challenges have emerged from this collective effort. The first is the need to employ the available resources to obtain the highestpositive impact on U.S. semiconductor technology. The second challenge is to interface with other organizations so as to assure that the SRC program is part of a broader strategy.

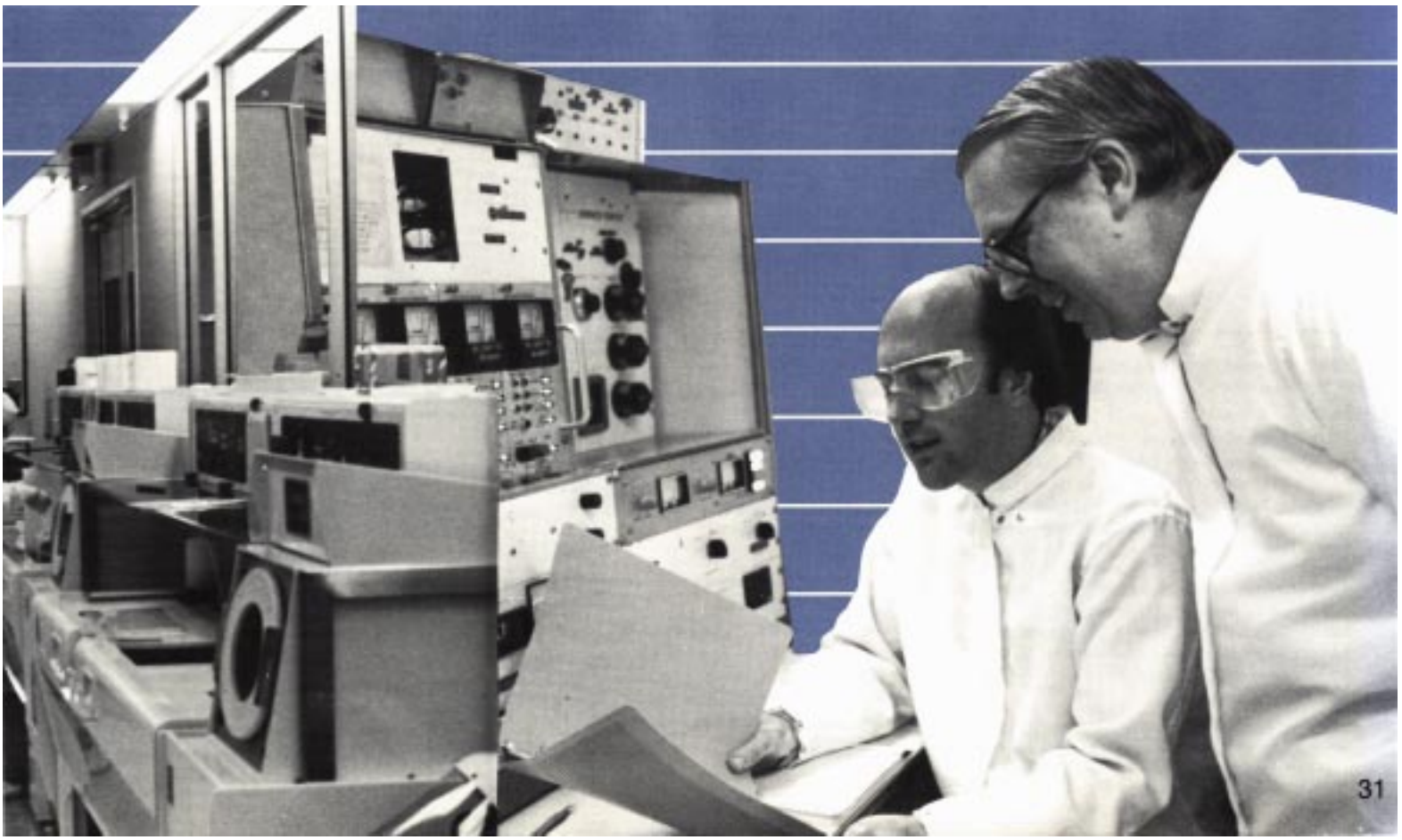
With respect to maximizing its impact on the U.S. technology base, the SRC has continued to refine its planning and forecasting skills, as well as its understanding of the role of university research. Evidence of this effort is distributed throughout this report. The challenge is to continue to refine the process by which the industry, government, universities, and the SRC staff carry out generic semiconductor research in order to increase the effectiveness of this team effort and to provide a more productive response to the need for a continuing flow of new knowledge, creativity, and innovation. Already, U.S. universities are the most productive in the world in their contributions to technology and science. Progress has been made in these management processes, and the productivity of the universities working with the SRC has increased considerably. However, more progress is required to meet competitiveness needs of the U.S. industry.

The roadmap for semiconductor technology in the U.S. is the central tool forplanning and forecasting. The combined technicalinput of the members is used to define technology advances over the next decade and to provide a basis for R&D investments. For example, the SRC research program is an investment designed to advance the achievement of certain future technical capabilities by U.S. industry. The impact of other investments can be related to the technology roadmap in a similar

manner, and the roadmap can be applied to the assessment of technology accomplishments in other countries. At present, this roadmap is incomplete. Only the quarter-micron CMOS branch exists at a detail level. Both for the purposes of the SRC and for the purposes of other efforts addressing the semiconductor technology base of the U.S., the completion of this technology roadmap must be given high priority by the SRC.

Knowing that the SRC is not alone in addressing the needs of the U.S. semiconductor technology base provides the challenge to work within an overall plan, i.e., a national semiconductor strategy. A large effort, amounting to over $2.0 billion a year, is devoted to semiconductor research and development in the U.S. A small percentage of this is generic research, and an even smaller portion is carried out by the SRC, approximately one percent of the total. Coordination between the SRC and other agencies funding generic research is growing, and the interfaces between generic research and the larger efforts in applied research and development are improving. At present, however, a national strategy does not exist. The SRC is participating in discussions with various bodies to evolve such a plan so as to increase the efficiency of all of the national efforts in semiconductors.

Photos: LEFT — Professor Toh-Ming Lu operating the Cluster ton Beam system at Rensselaer Polytechnic Institute; CENTER — the new Integrated Circuits Laboratory in the Center for Integrated systems, Stanford University; RIGHT — semiconductor research at North Carolina State University.



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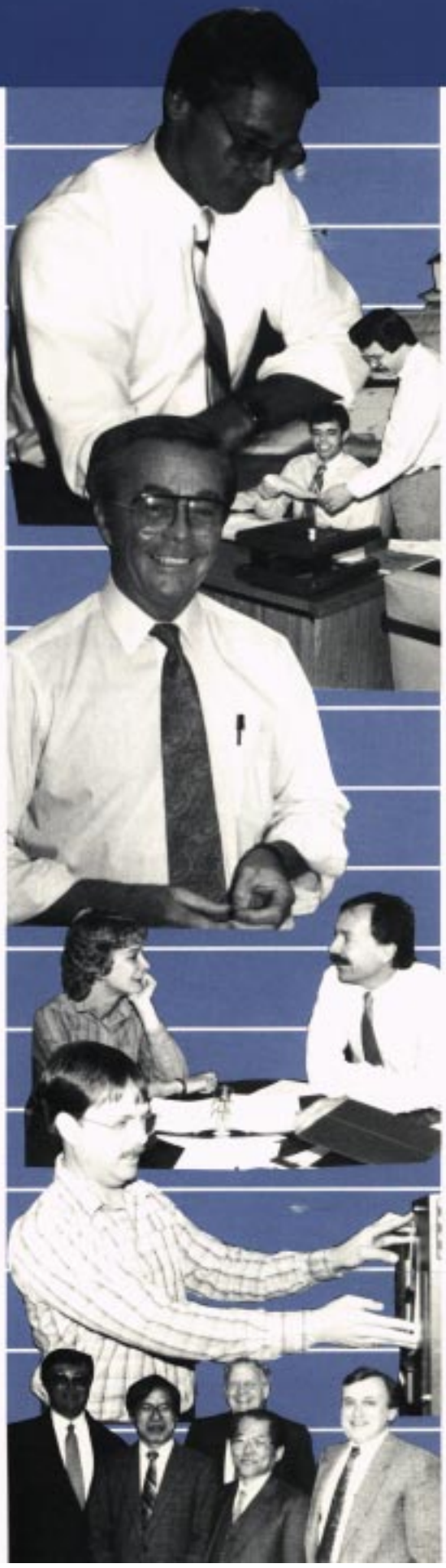

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