1984 ANNUAL REPORT

SRC

COOPERATIVE RESEARCH

SEMICONDUCTOR RESEARCH CORPORATION

Member Companies

COOPERATIVE
RESEARCH

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E.I. du Pont de Nemours & Company
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*The following companies are included in the Semiconductor Equipment and Materials Institute, Inc., CHAPTER: Micrion Corporation; Micronix Corporation; Pacific Western Systems, Inc.; Probe-Rite, Inc.; Pure Aire Corporation.

The Semiconductor Research Corporation is a consortium of US. companies having a common interest in accelerating the progress of research in semiconductor technology, broadening the university base, and increasing the supply of qualified personnel for the industry.

In February, 1982, articles were filed incorporating the SRC as a nonprofit organization to “conduct research which will include scientific study and experimentation directed toward increasing knowledge and understanding in the fields of engineering and physical sciences related to semiconductors.” The SRC assesses its members’ needs for research, develops strategies to meet these needs, and funds research that is consistent with these strategies.

The goals of the research are aimed at providing an advanced science and technology base leading to development efforts and subsequent industrial use.

Beyond these research goals, the SRC has a major responsibility for transferring research results to its member companies and in helping the United States maintain a lead in information technology.

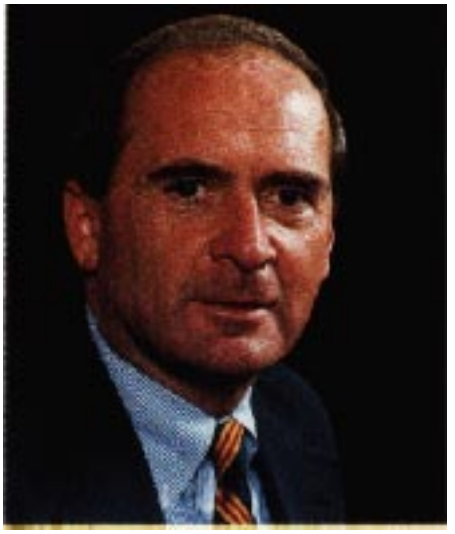
Although the technical program is primarily conducted at academic institutions, the SRC’s charter provides for undertaking exploratory and advanced development programs where and when appropriate to its goals and its members’ needs.

The SRC is currently supported by 40 U.S. companies who are either suppliers or users of integrated circuits, or vendors of material or equipment to the industry. The SRC’s Board of Directors is elected by the Semiconductor Industry Association and consists of executives from member companies. Two special advisory groups complement the board. The Technical Advisory Board, having representation from each member company, provides the Board and President with a continuing industrial perspective on the research program. The University Advisory Committee, drawn from senior faculty of representative U.S. universities, provides counsel on university relations, policies and practices.

— SRC Research, Microelectronics Center of N.C.

GEORGE M. SCALISE

Chairman,
Board of Directors



The SRC has completed its second full year of research funding. Having been involved since its inception, I have gained great personal satisfaction in the growth from the original eleven firms to the current 40. But even more significant, I have seen and felt the effects of the SRC on the university research community and on our industry. Two years is a very short time for a still relatively small operation to make this kind of impact. Through cooperative R&D, we are achieving together what we could not do separately!

The SRC was conceived as the U.S. semiconductor industry's response to the challenge of concerted national research efforts in other countries. Never has that challenge been greater. Since the SRC's formation in 1982, the share of the worldwide semiconductor market held by Japanese companies has increased from 33 percent to 37 percent. Worldwide market share for U.S. companies has dropped from 57 percent to 54 percent. In selected segments, such as memory, the picture is much worse. It is an ominous trend.

One of the strengths of U.S. manufacturers in worldwide semiconductor trade competition has been our ability to innovate. And it is imperative that we maintain that innovator's edge. However, the industrial community must take full responsibility for taking that innovation into our factories and to market rapidly.

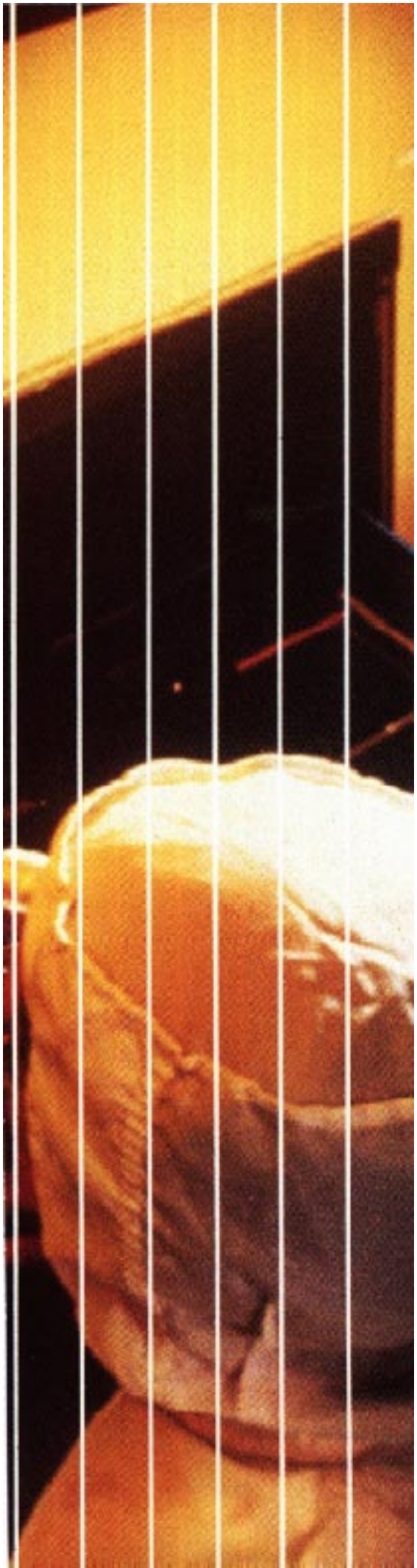
While we must be aggressive in putting new technology to use, we must be patient in terms of our expectations from long-term research. The research we support looks far into the future. Its purpose is preservation of our species. We cannot, and should not, expect short-term miracles. It is also important to remember that we are getting a combination of research results and highly trained manpower. If we wanted either one alone, we would have done it another way.

Although not discussed in this report, a large amount of effort was expended by the SRC technical staff in preparation of an industrial research initiative: Project Leapfrog. For a variety of reasons this ambitious program was not initiated in 1984. We are continuing to evaluate options that would allow us to address this type of effort without dilution of our university research program.

I would like to share with you my vision of 1995 and the effects the SRC will have had on our industry by that time.

> The US. semiconductor industry will cross the $100 billion/year level. This industry will be using many of the devices, processes, concepts, and software that are currently being researched through SRC contracts. Over 3,000 professionals who were supported by SRC-sponsored research will be employed in our industry, actively producing products and developing new ones. At least 50 universities will be producing highly qualified undergraduate and graduate microelectronic engineers and scientists, at least 20 of which would not be involved except for SRC support. Over 1,000 graduate students and 300 faculty will be engaged in SRC research. The SRC scheme of cooperative research will have been emulated by other industries, and a majority of their academic support will flow through such cooperatives. The government will recognize the role of the research cooperative and will funnel increasing percentages of its research funds through these industry-directed efforts.

I would solicit your help in continuing to provide the SRC with the necessary resources to make this happen, We are a cyclical industry, but we must not let short-term influences determine our long-term future. I know that we are capable of meeting the challenge.



LARRY W. SUMNEY

President

The forty companies that comprise the current SRC membership represent the bulk of U.S. capability in integrated circuits and their application. These companies belong to the SRC for a variety of reasons. All of our members recognize the decline in U.S. competitiveness and the need for changes in the way we do business — like cooperative R&D. Even the U.S. Government's Office of Technology Assessment is questioning who will fill the role of a surrogate national laboratory for microelectronics and information technology. Many members with small research organizations, concentrating on near-term products, recognize the need to invest in a longer range program. Others with significant internal R&D efforts regard the growth of university faculty and a continuing stream of qualified graduate students as a major interest. Still others emphasize directing the attention of the academic community to areas such as manufacturing which have been traditionally neglected. Trading off these various interests at current budget levels involves quite a balancing act.

In 1983, the Board of Directors encouraged us to begin to broaden this country's university base in microelectronics by funding research at schools that do not yet have an established reputation in this field. This was supported by our University Advisory Committee, and today we have contracts at 16 schools in this category. This is necessary if we are to have students needed for industry and the faculty necessary to train them. These seed efforts have resulted in significant leveraging of our funds through grants by federal and state agencies — as much as 3:1 in some cases. At the same time, we see the need to concentrate programs requiring state-of-the-art capital equipment at major centers where costs can be shared and the faculty exceeds a critical threshold size.

You will note in this year's report, a continuing change in emphasis and direction in some of our programs as problems are solved, priorities shift, and new opportunities arise. Next year will see increased emphasis on manufacturing and process research — fields in which the universities must become more involved.

The growth in understanding between industry and university that is occurring as the result of interaction among our members, faculty and graduate students is most rewarding. Except in a few instances such as national defense and space, the United States has been relatively ineffective in mobilizing the academic community. I feel that through the SRC we are beginning to demonstrate that industry and academia can work together on solutions that are crucial for the economic survival of the commercial U.S. integrated circuit industry.

Various government agencies have expressed an interest in an appropriate relationship with the SRC. Although nothing is solidified, I would expect this situation to be resolved in the coming year. It is also heartening to note that several of the recommendations of the President's Commission on Industrial Competitiveness describe the type of cooperation embodied in the SRC.

In 1982, an estimated $70 million was provided to universities for integrated circuit research but only $7 million was associated with silicon — the backbone of our industry. In 1984, we estimate that $23 million will be spent on silicon research at universities, more than half of which is supplied directly by the SRC.

The SRC is beginning to make a difference!

Photo Courtesy of General Electric Company

1984 Research Funding

Microstructure Sciences	$5,801,574
Manufacturing Sciences	$3,544,888
Design Sciences	$3,974,845

— SRC Research, University of California at Santa Barbara

RESEARCH

"Setting Long-Term Goals For The Semiconductor Industry"

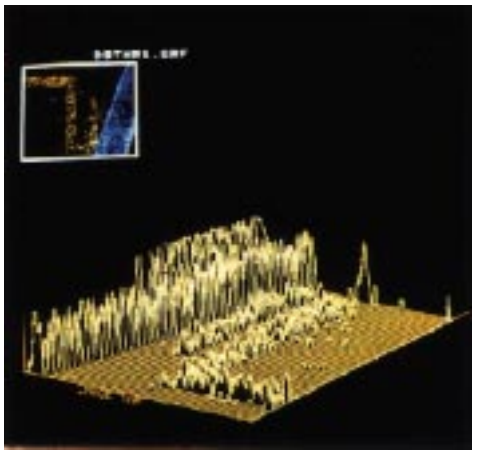
The U.S. semiconductor/computer industry has established the SRC as the organization through which it sets research goals and future directions of the technology. This is accomplished jointly by the SRC Technical Advisory Board, its working committees, and the SRC technical staff. These directions are then translated into relevant university research programs by the SRC which subsequently monitors and guides the research progress, interprets and disseminates the resultant scientific information and, where applicable, transfers technology to the member companies through appropriate vehicles.

Starting in 1982 with a budget of $6 million, the research program has expanded in scope and direction. In 1984, over fifty research contracts totaling $12 million were in place at 37 universities. Currently, more than 180 faculty and 400 graduate students are involved in SRC contracts. The program addresses needs for improved performance and higher density integrated circuits with increased reliability, designed in short cycles to be free or tolerant of faults, easily tested, and produced by controllable manufacturing processes at acceptable costs.

On a more quantitative level these goals read; "by 1994 we shall be able to:"

- increase complexity 250 fold
- increase performance 10,000 fold
- decrease cost/gate 500 fold
- maintain chip reliability of no more than one failure in 10 million hours.

These goals must be reached with full consideration given to the additional factors of capital costs per unit area of silicon, wafer throughput and automation, disposability of reaction products, defect introduction, stability of processes, safety, and increasing wafer size.



Pseudo Three-Dimensional Display of EBIC Image of IC Sructure
—SRC Research, University of North Carolina

— SRC Research, University of California at Santa Barbara

MICROSTRUCTURE SCIENCES

Goals

Microstructure Sciences research encompasses materials, phenomena, devices, circuits, and techniques required to achieve the industry's 1994 complexity and performance goals:

- 2×10^7 transistors/cm^2
- 50 pico seconds logic gate delay
- 5 femtojoules power-delay product
- 16-bit analog-digital converter at 100 MHz.

These goals are being addressed through a major effort on the identification and solution of key problems limiting the development of a 0.25 micrometer CMOS technology, and through four complementary efforts on optical interconnect, multilayer integrated circuits, high-speed submicron bipolar technology, and III-V high electron mobility transistor/heterojunction bipolar integrated circuits. Feature size will continue to decrease, four levels of interconnect will be required, and new concepts will be needed to overcome the circuit speed limitation imposed by today's interconnect technology.

0.25 Micrometer CMOS

CMOS circuits have the inherent advantages of low-power dissipation, improved transfer characteristic, greater resistance to soft errors, and enhanced noise immunity. Coupled with a manufacturing cost near parity with NMOS for advanced complexity ULSI components, CMOS has become the MOS technology of choice for the VLSI/ULSI era. Device modeling has shown that MOS gate lengths of about 0.25 micrometer are the practical scaling limit as contact resistance, interconnect delays, and, eventually, reliability, will limit further size reduction The SRC 0.25 micrometer CMOS research thrust is centered at Cornell University, with contributing projects at Wisconsin, Illinois, Stanford, Colorado State, Arizona, Yale, and Notre Dame where particular expertise exists.

During this past year several key processes, models, and fundamental physical effects have been elucidated. A 0.5 micrometer minimum feature size process employing E-beam patterning has been demonstrated, and 0.25 micrometer minimum feature size MOS transistors have been fabricated. Device models have been formulated which include the effects of ballistic transport in short-channel devices. Selective deposition of tungsten by LPCVD has been demonstrated to produce high-quality Schottky diodes suitable to fabricate latchup-free CMOS. $MoSi_2$ and WSi_2 deposited from hot-wall CVD reactors, and SiO_2 and SiO films produced from ion cluster beams, have been shown to have acceptable film quality. A new protonic interface trap has been discovered and identified, and an ion implantation process has been developed and characterized which inhibits the lateral encroachment of silicide in small silicide contact areas. Integration of these important elements into a total CMOS process will begin in the coming year.

Optical Interconnects

A potential solution to both interchip and intrachip communications delay is optical interconnect. Ill-V light emitters and silicon photodetectors integrated on the silicon wafer are one possibility with interlevel dielectric acting as an optical wave guide. MBE and MOCVD techniques are being pursued to fabricate $Ga_xAl_{1-x}As$ quantum-well, light-emitting devices on silicon substrates as an optical interconnect source. GaAs light-emitting diodes integral with silicon have been made.

Multilayer Integrated Circuits

The potential for multilayer integrated circuits is being explored in the SRC research program at MIT. The thrust of the effort is to produce single-crystal silicon films on non-crystalline substrates at low temperature, and to fabricate integrated circuits in these films using low temperature processes. Although a new method (surface-energy-driven secondary grain growth) for producing large crystals has been developed, it does not appear that usable single-crystal films of sufficient area in 750-angstrom-thick layers can be produced below a temperature of 800°C. P-channel MOSFETS, fabricated as the second-level transistor of a joint CMOS gate inverter were made using a composite Si_3N_4 on SiO_2 gate dielectric. The devices have a leakage current dependent on gate voltage due to field-enhanced emission.

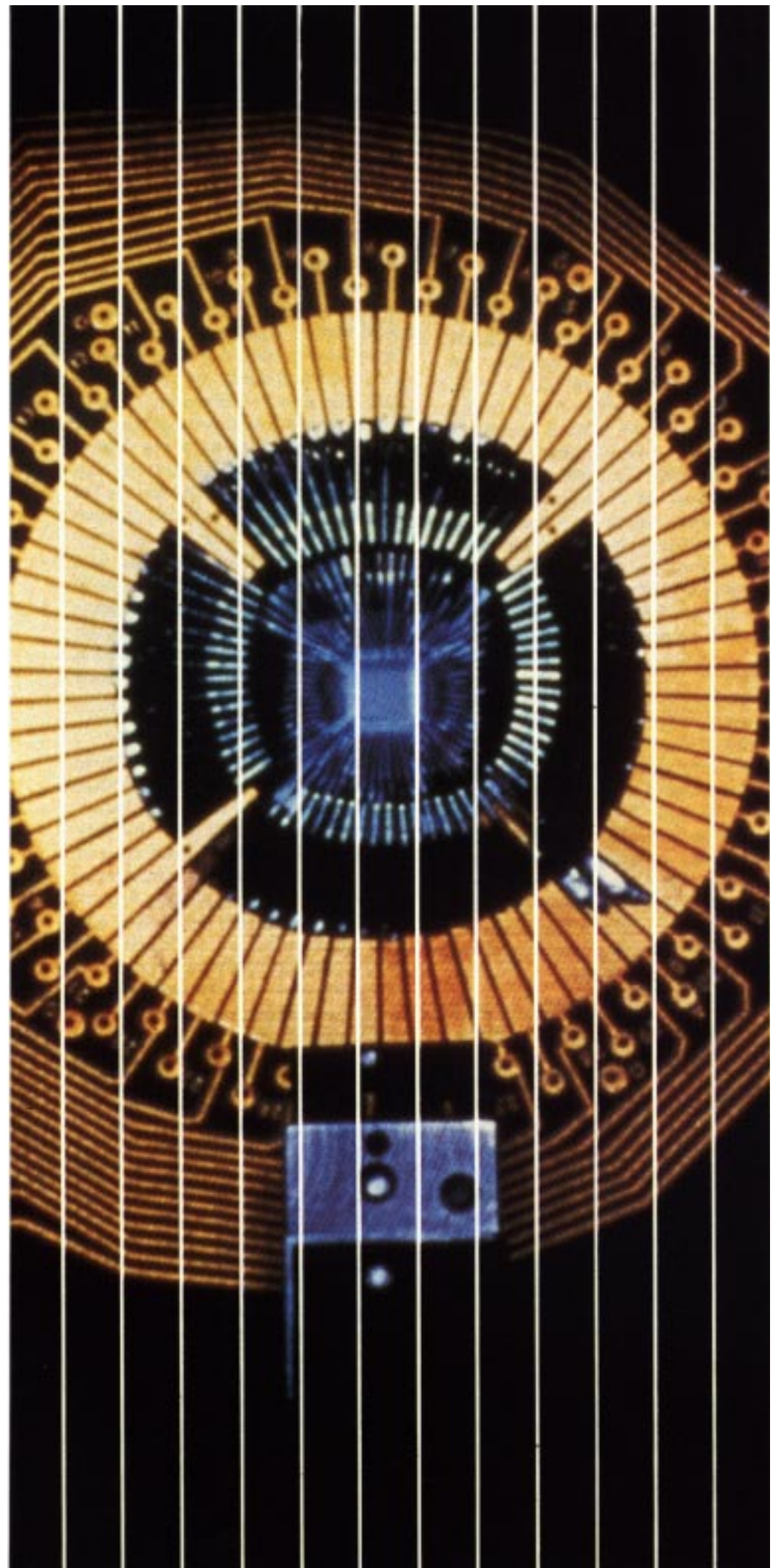
High-Speed Bipolar Devices

Although CMOS technology is favored for ULSI circuits, bipolar technology remains important for high-performance analog and high-speed digital applications. For CPU applications, package design can accommodate the power dissipation requirements of emitter-coupled logic circuits. Logic circuits that combine CMOS FET's with bipolar transistors can operate at subnanosecond speeds but only dissipate the fractional milliwatt power level of CMOS. Bipolar totem pole drivers, fully oxide-isolated with sidewall base contact and polysilicon emitters, can drive the off-chip capacitive loads. Polysilicon emitter research is underway, and additional projects in bipolar/CMOS and high-speed bipolar technology are planned.

I I I-V Digital Devices

Ill-V technology, in addition to its well-known, band structure dependent properties of direct band gap optical photon emission and high mobility, provides a flexibility to build devices using artificially structured material that is not available in silicon. Recent research in quantum-well lasers and high electron mobility transistors has taken advantage of these properties. A joint effort between the University of California at Santa Barbara and Stanford University is conducting HEMT/HJBT device research. The basic difference between HEMT and MESFET devices has been explored in terms of electrostatic potential that causes a saturation of the diffusion velocity rather than the drift velocity. A HEMT SPICE model has been developed, and the use of superlattice structures under the gate has been investigated to eliminate deep levels in the n-AlGaAs barrier layer. MBE growth stop-and-restart capability has been demonstrated using InAs as a passivating layer.

The guidance of the Microstructure Sciences Subcommittee has been invaluable in the formulation and the review of SRC research programs during the past year. The research has been high quality and productive.



Goals

The research goals in Design Sciences specify that a chip at 1994 levels of complexity (2 x 10^8 transistors) should require no more than six man-months of design effort to map from high-level description to error-free layout. In addition, the resulting design must be economically testable to assure less than 1 in 10^6 rejects. This design productivity goal exceeds current capability by several orders of magnitude, and the design fortestability goal is much more aggressive than the 'fault coverage' metrics often used for testability today. A more subjective goal is the development of new architectures that provide enhanced processing and memory capabilities, IC technology is becoming increasingly I/O, and interconnect limited and novel architectures may offer alternative solutions. Workstations having two orders of magnitude more computational power are needed to support design using next generation levels of IC complexity. Moreover, the design process must be moved to higher levels of abstraction in order to increase designer productivity.

SRC research in design methods includes work in device and process modeling. physical design, synthesis methods, design verification, design for fault tolerance and testability, and new design concepts for VLSI architectures In 1984, a Request For Proposal was issued to expand effort in design concepts.

Photo Courtesy General Electric Company

DESIGN SCIENCES

Physical Design

The physical design problem is one of the most important IC design tasks since it deals with the placement of macrocells on the chip and the subsequent interconnection of the macrocells according to a given net list. An effective solution minimizes both the chip area and the length of interconnects between the macrocells and thereby enhances yield and performance simultaneously. Approximately 15 tasks were underway in 1984 in the SRC Design Sciences research program across a wide spectrum of algorithms and design styles, Examples include: TALIB, an NMOS cell layout system based on knowledge engineering principles; algorithms based on eigenvalue methods for graph bisection; probabilistic search methods for layout using the simulated annealing paradigm; fast and efficient PLA folding software; and fundamental channel routing studies. SRC graduate students also contributed to larger projects such as MAGIC and BBL.2. The latter two programs are now available to U.S. companies from the SRC Center of Excellence in IC/CAD at the University of California at Berkeley.

Device and Process Modeling

The need for accurate models for short channel MOS devices as well as extraction methodologies to determine parameter values from process measurements has served to motivate the development of the BSIM project at Berkeley. If one accepts the view that the actual manufacturing process for IC's is characterized by statistical disturbances that create variations in IC device parameters, then analysis tools are needed to predict the impact of process variability on the circuits' performance. The FABRICS-II software tool set has been developed at the SRC Center of Excellence in IC/CAD at Carnegie-Mellon University to allow evaluation of the impact of process statistics on design. Process models such as those used in FABRICS are also providing impetus to the study of optimization methods for both circuit and manufacturing control system design.

Design Synthesis

It has been clear for some time that the designer should enter the design process at a higher level in order to increase productivity. However, most past attempts fall short with respect to both levels of abstraction and density of design. The design automation effort at Carnegie-Mellon has several projects that address elements of this problem, including: DEMETER, a high-level design aid for a computer system on a chip; a chip interface synthesis project; MOBY, a module binder that associates hardware with data paths; ULYSSES, a CAD knowledge-based advisor for tool utilization; and CLEOPATRA, a natural language interface for circuit simulation. In addition, several other tasks are underway that focus on other specialized synthesis applications: analog-digital signal processors; silicon compilation from Boolean equations based on level graph heuristics; UNIGRAFIX, aflexible graphics interface software system; and hardware compilers based on the gate matrix design style.

Design Verification

After an IC layout has been completed, there remains the very important issue of verifying that the circuit is error-free and that it achieves the intended functional and performance goals. SRC research tasks in design verification include circuit simulators (BIASlisp, a Lisp-based circuit simulator; RUBICC, an expert circuit critic), timing simulators, logic simulators (E-Logic), design rule checkers, circuit extractors, and a layout profile predictor for use in estimating device characteristics from process parameters and flow (SIMPL2). Software systems are sometimes complemented by the use of hardware accelerators for verification. At Berkeley, a multiprocessor system has been shown to reduce circuit simulation time relative to a comparable single processor system.

Design for Testability

The testing of integrated circuits to assure that they are fault free to the degree required by the 1994 goal set is very difficult and may require lengthy and expensive test procedures. In the new SRC Program in Reliable Chip Architectures at the University of Illinois/Urbana-Champaign, several facets of the design-for-test problem are being addressed. Tasks include: (1) software to automatically generate test patterns for a wide class of microprocessors, (2) built-in self test for microprocessors, (3) fault simulators that efficiently evaluate the effectiveness of test procedures, and (4) fault tolerant design procedures for highly concurrent matrix and signal processor computing arrays. Other research tasks include: VICTOR II, an automatic test pattern generator for digital circuits; PLATEST, a generator of automatic test patterns and/or self-test circuitry for PLA's; concurrent on-line testing schemesfor microprocessors; testable CMOS speed-independent circuits; and a new technique called Inductive Fault Analysis that relates physically occurring process defects to circuit faults.

VLSI Architectures

Another major area of research is novel architectures and applications for IC technology. Two processor design projects — CONDEL (CONcurrent Directly Executed Language machine), and MISP, (Multiple Instruction stream, Shared Pipeline processor) — are currently being supported. A 20 nanosecond pipelined floating point processor is being designed using the very dense NORA CMOS Technology. This effort will be expanded in 1985.

This country has a lead in design sciences. The SRC is fortunate to have involved in its programs a number of world-recognized universities and researchers Universities are an ideal place to conduct research in design sciences, and the results of this research can often be rapidly transferred to industry. The dedication of the Design Sciences Subcommittee has contributed in a major way to the effectiveness of this program.

MANUFACTURING SCIENCES

Goals

The purpose of the Manufacturing Sciences research program is to develop a generic technology base that addresses the effective use of technical, economic, and human resources in optimizing production capabilities for integrated circuits at the cost and with the quality required. Because the manufactuing sciences have not been part of academic research agendas, much effort is required to define and initiate a research program where none previously existed. inherent in the program is the development of means to attract high-quality graduate students and faculty to semiconductor manufacturing sciences. Packaging and reliability, both of which suffer from a similar lack of university attention, are included as part of the manufacturing sciences effort.

The ten-year goals of the SRC Manufacturing Sciences research program are to create manufacturing capabilities for the 1994 complex chip technologies defined in the microstructure sciences program. This requires reducing defect levels to 0.25/cm^2, developing process capabilities and automation that enable five-fold improvements in productivity, and keeping capital costs at acceptable levels, The performance of high-speed digital circuits is already limited by packaging from both a thermal and electrical viewpoint, and the goals of 100 watt packages with 400 I/O's and port•hertz products of 10^{12} are probably conservative. Current levels of reliability with a 250-fold increase in the number of devices/chip must be maintained.

Fabrication Technology

The core Manufacturing Sciences research program consists of three related efforts at the Microelectronics Center of North Carolina (MCNC), Stanford University, and the University of Michigan.

The program at Stanford is focused on modeling and simulation of equipment and unit manufacturing operations directed toward the evolution of more efficient CAM/CAF tools and the management of yield. The initial year of this research has concentrated on automation, micropattern generation and inspection, etching, device and process modeling, and testing and yield modeling. The automation research centers on the development of a representation language, FABLE, for fabrication operations. A sensitive electrical end-point detection method for plasma etching has been demonstrated, and a defect reduction scheme for lithography using successive exposures through different but identical reticules has been developed.

At Michigan, SRC research is directed to automation of selected semiconductor unit operations. Reactive ion etching is the initial research vehicle. In-process sensors, testing, machine vision, expert systems, and modeling are the subjects of research during the first year. A thermal imager, an integrated gas flow controller, and an automated process cell controller are being developed.

MCNC is integrating a low-temperature, 1.0 micrometer CMOS fabrication capability. The scaling of vertical doping profiles and lateral lithographic dimensions is being approached through tasks on shallow junction formation, extrinsic gettering, plasma contamination and damage, and plasma-assisted oxidation. The fabrication related research is addressing the effects of particulates, CMOS latchup, and process integration. It has been found that B+ implants are preferred over boron fluoride ions and that implant channeling necessitates precise wafer orientation control. Leakage current in shallow p^+/n junctions can be reduced significantly by a two-stage annealing procedure: a low temperature preanneal followed by rapid thermal annealing. The incorporation of germanium during epitaxial growth to obtain misfit dislocations has been successfully demonstrated for impurity gettering. In the particulate area, measurements have been made in clean rooms down to 10 nanometer particle diameters, and current research is focusing on the study of particles on wafers.

Reliability

A research program directed to the reliability of submicron integrated circuits is underway at Clemson University. The three tasks are electromigration, charge trapping, and electrostatic discharge. During the initial period of this research, emphasis has been placed on expanding the university's instrumentation and analytical capability.

Packaging

A major effort in packaging was initiated at the University of Arizona in 1984. The goal of this work is a computer modeling and simulation scheme for first-level packages based on interactive thermal and electrical considerations. Several existing modeling schemes have been evaluated for their applicability to packaging. Particular emphasis is being placed on the inductive switching noise and transmission line problems in high-speed circuits, The program at Stanford on enhanced cooling techniques for VLSI produced the first technology transfer for SRC research with at least two member companies proceeding with advanced development activities. Thermal dissipation of 1400 watts/ cm^2 was demonstrated in silicon through the use of liquid-cooled microchannels. This work has led to other applications on capillary hold-down of wafers in vacuum and improved die attach. The Cornell activities on defects in multilayer ceramics is leading to models for controlling shrinkage for composites used in complex packages. A new project on hybrid wafer-scale integration, which involves a silicon wafer as an active

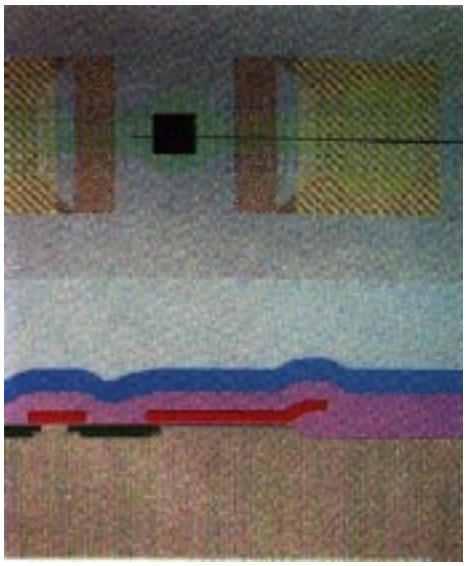
package substrate, was initiated at Auburn University. A Packaging Strategy Committee composed of experts from twelve member companies has been instrumental in developing a plan for increased university attention to packaging sciences. Five universities will participate in study contracts leading to a major new program in 1985.

Metrology

At the University of North Carolina, work with digital scanning electron microscopy has resulted in a new technique (PREBIC) which has been applied to the analysis of current-related phenomena in CMOS devices. The acoustical microscopy project at Minnesota continues to evaluate the utility of this instrument for nondestructive analysis of subsurface VLSI structures.

Manufacturing sciences represents the SRC's biggest challenge. It combines the largest need expressed by industry with a major void in academic research to date. It is further complicated by the fact that the technical literature does not represent state-of-the-art industry practice, thus dictating a diligent educational and motivational effort by experts from member companies directed to university scientists.

Photo by Tom Tracy; Courtesy of Advanced Micro Devices, Inc.



CAD Simulation of CMOS Inverter
Cross Section Using SIMPL-2
— SRC Research, University of California at Berkeley

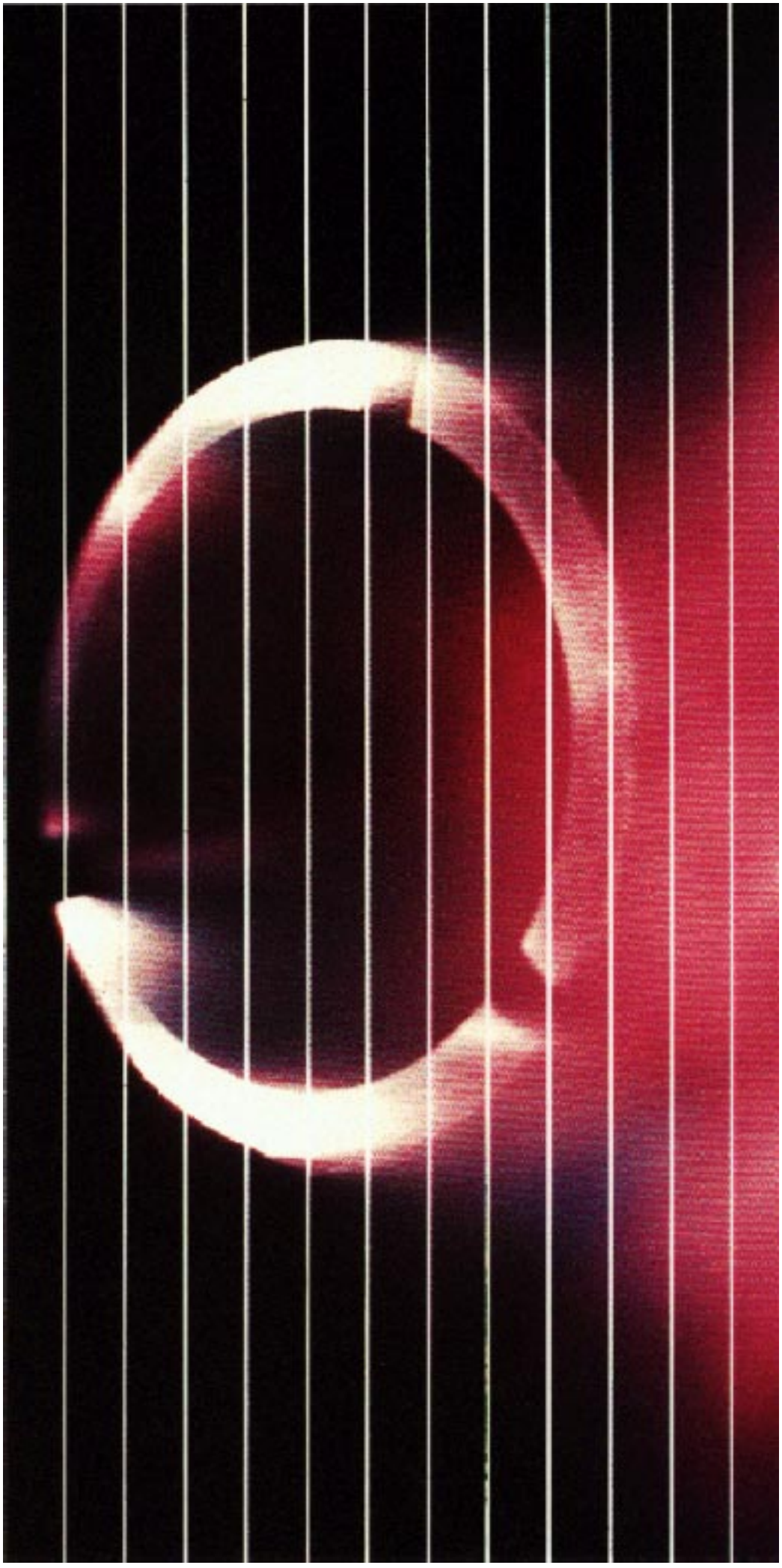


Photo Courtesy of Eaton Corporation

FUTURE DIRECTIONS

Goals

By continuing refocus of established research thrusts, the SRC is addressing the near-term needs of its member companies. New thrusts are directed to longer range research in the ten-year time frame. Three areas are presently identified, with funding planned and initiated: "post-shrink" silicon devices, *in-situ* manufacturing, and system design concepts.

"Post-Shrink" Silicon

The feasibility of building computing structures of higher performance and complexity than can be accomplished at the limit of 0.25 micrometer silicon IC technology has recently been defined by the SRC in a "Post-Shrink" Silicon Workshop. Through the use of artificially structured materials, systems of reduced dimensionality may be fabricated which exhibit quantum domain phenomena. Distributed computer architecture systems, consisting of quantum-coupled oscillator arrays, may then be envisioned. Principal contributions to the "post-shrink" thrust are being made at Cornell and the University of California at Los Angeles. A theory for the band structure of two-dimensional (patterned), ultra-small, periodic superlattice structures has been developed; and, three-terminal device structures based on a superlattice construct have been conceived. Additional projects are planned.

In-Situ Processing

As the sophistication of computer-aided design tools for the rapid design of integrated circuits and integrated circuit complexity increases, a greater portion of the circuits manufactured will be custom designs. Artificial intelligence applications that require several orders of magnitude more logic and memory than provided by the current generation of custom designs and accelerators can be identified. This use of custom circuits impacts the approach for future manufacturing systems; i.e., high-yield, short-cycle-time fabrication (based on *in-situ* processing in which the wafer is maintained in a stable environment and processes are brought to the wafer) will become increasingly important. The SRC is establishing a thrust to develop an *in-situ* technology that addresses this future need. Research programs employing energy beam processing are underway at Rensselaer Polytechnic Institute, the University of Illinois, the University of California at Los Angeles, The Johns Hopkins University, and Columbia University. A time-dependent general model describing the incorporation of dopants into single-crystal films grown by MBE has been developed. Prior to attempting to fabricate superlattice structures, growth of laterally uniform $CoSi_2$ on silicon by MBE has been achieved.

Design Concepts

Algorithm design, system architecture, concurrency of operation, and device technology are the major avenues along which computer science and engineering have traditionally pursued their central goal of increasing computational throughput. In the past, algorithm design has sought to develop better procedures and data structures that will reduce the time to solve specific problems on a given computing system; concurrency of operation has sought to achieve a better utilization of available resources by overlapping activities that use disjoint parts of the computing system; device technology has advanced along the traditional lines of reducing the minimum geometries; and, system architecture has constructed the hardware resources to optimize the system for classes of algorithms. Increasing complexity and design capability mean that architectures specific to a given algorithm are affordable through custom design. Recognizing this, the SRC has initiated a thrust to investigate and develop advanced architectures that will address identified future applications.

In late 1984, the SRC began a search for innovative design concepts for the ULSI/VLSI generation of technology by issuing a Request for Proposal to the university community. As a consequence of this solicitation, new research will be started in 1985 in computing arrays for large chips, high speed/accuracy analog-to-digital conversion, and new built-in test design methods. The SRC is continuing to expand its initiative in the design concepts with research in signal processing architectures, adaptive associative memories, and artificial intelligence engines.

OUTREACH

Goals

The activities of the SRC are providing an opportunity for technical professionals and managers to become involved with university researchers, often for the first time. Participation in technical committees, conferences, and workshops are vehicles for interchange not found in the large professional societies, Following are some of the highlights that characterize this increasing involvement and commitment of the members.

Technical Advisory Board and Subcommittees

The Technical Advisory Board (TAB) continues to be the major focus of interaction and information exchange among industry, the SRC staff, and the universities. Participation in the Technical Advisory Board and its three subcommittees doubled in 1984 with the opportunity for each member company to be represented on each subcommittee. The addition of nine new member companies during 1984 brought new expertise and perspective. The first SRC-TAB planning session held in August resulted in changes in scope and direction of the research program and further quantified the technical goals for the 1990's. This annual "summer study" provides continuity in TAB leadership.

Industrial Mentor Program

The Industrial Mentor Program in which technical experts from member companies affiliate with individual university research tasks as resource people is unique to the SRC. This program is the result of recognition by the Technical Advisory Board that the university benefits from continuing industrial perspective and resources. Layouts, mask sets and custom fabrication of wafers are examples of services offered to universities by members At the request of the TAB, the number of mentors was increased from 55 to 145 during the year. This was applauded by the university community. The mentors gain from real-time interaction with faculty and students performing research relevant to their special interests. Opportunities for additional mentors will continue to grow as the research program expands.

Topical Research Conferences

Topical Research Conferences deal with a specific topic that is part of the SRC's ongoing research. They create an environment for active dialogue among researchers in the field. Many purposes are served: early access to research results, inputs from unpublished industrial research efforts, and constructive critique. During 1984, conferences on the following subjects were held:

Built-In Testability
VLSI Interface Engineering
Design Synthesis
Devices and Structures
Manufacturing Sciences
Interconnections and Contacts
Rapid Thermal Annealing

Attendance, limited in order to encourage interaction, averaged 45 persons per meeting. Over 285 different representatives from member companies and faculty participated. The conference on Rapid Thermal Annealing was judged by leading researchers as the best forum ever held on the subject.

Workshops

Workshops help the SRC decide whether a new research thrust is appropriate and where the most fruitful approaches lie. Leading researchers are invited from industry, government, and academia to present historical perspectives, current research, and views of technology limits and opportunities. For the Wafer-Scale Integration Workshop, survey papers written by commission of the SRC reviewed the history of worldwide research on this subject while active industrial and university researchers provided a cutting edge view. The conclusions were used to formulate beginning projects in the new in-situ processing thrust. Workshops on "Post-Shrink" Silicon, Health and Safety, *In-Situ* Processing and Technology Assessment are scheduled for 1985.

Technology Transfer Courses

The product of research is understanding and sometimes invention, while technology is usually the result of development. Since the SRC is not yet engaged in development, the task is to assist the universities in interpreting the significance of their research and in defining what needs to be done by industry to develop technology. In the case of software and analytical techniques, a direct translation can often be made from university research to industry use. An effective way to accomplish this for the member companies is through short courses given by the researchers themselves, The first Transfer Course, FABRICS-II, was held at Carnegie-Mellon University. Due to limitations imposed by laboratory facilities, attendance was restricted. Repeat sessions will be scheduled to meet all members' needs. Three additional courses are scheduled for 1985:

Microstructure Characterization Techniques — Cornell
Ill-V HEMT Modeling — Stanford
Analog Design CAD — Georgia Tech

A continuing stream of these events is anticipated as the SRC research programs progress.

Publications

Publishing activities increased dramatically in 1984. The library now contains 800 documents including contract reports and papers, the Technical Report Series, proceedings of SRC conferences and workshops, and newsletters Twenty-one company libraries have established procedures to archive and distribute SRC information. In addition to regular mailings, individual requests are being received at the rate of over 400 per month — most of which are filled within 48 hours.

Information Central

Over 125 people now have direct access to our VAX 11/780 Information Central system. The primary activities are electronic mail and requests for

publications. New features are being added as this computer capability is upgraded.

The user base will increase as software support for a variety of terminals becomes available from the SRC. Portions of the SRC data base are now on tape and available to members for incorporation into internal information systems.

Researchers in Residence

Opportunities are provided for researchers who are employees of member companies to hold visiting research faculty positions at universities that are participants in the SRC program. Applicants must be approved by the university, and the residencies are typically six months to two years.

Speakers Bureau

Effective in March, 1985, the SRC Speakers Bureau will begin operation. Over forty university researchers under contract to the SRC will be available as visiting lecturers to member company locations. Eighty topics are included. This program provides company audiences the opportunity to review research and to discuss issues of particular relevance to their business.

Industrial Residency at the SRC

The SRC provides the opportunity for member companies to place Program Managers on the SRC Technical Staff for periods of one to two years. This residency program seeks employees with management and technical expertise in specific fields of interest to the SRC to lend industry perspective to the research effort and to help with the task of monitoring research contracts To date, seven specialists from five companies have participated.

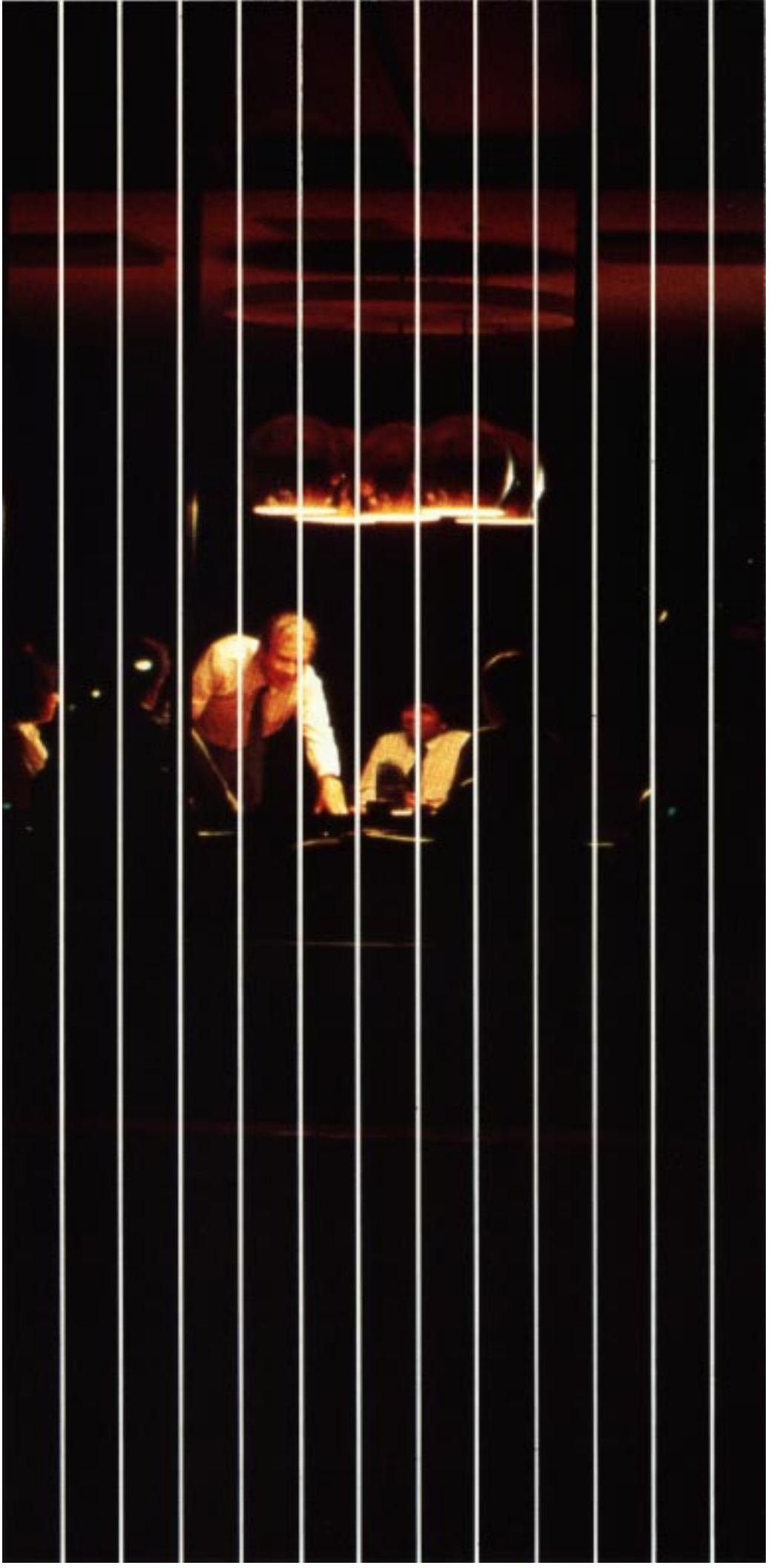


Photo by Tom Tracy; Courtesy of Advanced Micro Devices, Inc.

1984 RESEARCH PORTFOLIO

Arizona, University of

Chemical Vapor Deposition of Refractory Metals and Their Silicides From Solid Sources

Efficient Method for Simulating MOS Integrated Circuits and Its Implementation in Currently Used GAD Tools

Electrical Modeling and Simulation of VLSI Packages

Thermal Modeling and Simulation of VLSI Packages

Experimental Characterization of VLSI Packages

Arizona State University

A Three-Dimensional VLSI Device Simulator

Auburn University

Active Silicon Wafer-Scale Packaging Technology

Brown University

Hierarchical Silicon Compilation

California at Berkeley, University of

Goal-Oriented Hierarchical Building-Block Layout System

Routing Region Definition and Ordering

Gridless Channel Routing

Routing in MAGIC

YACR-Yet Another Channel Router

Topological Design of Array Logic

Theoretical Analysis of Probabilistic Hill Climbing Methods for Layout of Integrated Circuits

Graph Bisection Using Multiple Eigenvectors

Global Wire Routing in Two-Dimensional Gate-Arrays

Electrical Logic Simulation

Object Oriented Programming in BIASlisp

BLOSIM

SIMPL-2 (SIMulated Profiles from Layout — version 2)

BSIM, an IC Process-Oriented MOSFET Model and Associated Characterization and Simulation Facility

Nonlinear Device Validation: Hardware and Software Aspects

Characterization and Modeling of Intrinsic and Extrinsic Gate Capacitances of Small-Geometry MOSFETs

Scalable, Process-Independent Analog Macrocells for Analog-Digital VLSI

Expert Systems for Circuit Verification

Software Aids for Programmable Digital Signal Processors

Flexible Manufacturing Cells for CAM

DELIGHT.MIMO: An Interactive, Optimization-Based Control System Design Package

Information System for a Microfabrication Facility

Low-Pressure Hot-Wall Silicon Epitaxy

Control of Dopant Diffusion in Silicon Dioxide

Stress-Strain Analysis of Oxidation Process for Advance Isolation Technologies

Antialiasing and Realistic Rendering

Applying Color Science to Raster Computer Graphics

Berkeley UNIGRAFIX

Testing for Regular Structures and Self-Testing Techniques

Testability Analysis of Digital Circuits

Testability Analysis for Analog Circuits

Software Reliability

MOS Model Implementation in Next Generation Circuit Simulation

Transistor Models for BIAS-B/P

Bagel: Berkeley Automatic Gate Array Layout

Automated Parameter Extraction System for the CSIM MOS Device Model

Optimization-Based Design of Robust Control Systems

Robot Programming and Inverse Kinematics

Hand-Eye Coordination Problems for Robots

Computer-Based Precision A/D Converter Testing

Floating Point Support for Special-Purpose Simulation Hardware

California at Los Angeles, University of

MBE of Silicides for VLSI Applications

California at Santa Barbara, University of

Device Physics of III-V Heterojunction Field-Effect Transistors

Optimization of III-V Heterostructure Configurations

Laterally-Structured, Multiple-Level MBE Capability for Ill-V Devices

Carnegie-Mellon University

An interactive Graphical Process Editor for FABRICS-II

A Methodology for Optimal Test Structure Design

Analytical Modeling of Small Geometry MOSFET's

Parameter Estimation for Statistical Process Characterization

PROMISE — A Fabrication Process Optimization System

Interface Specification and Synthesis

DEMETER Project — DA Design Aid for Integrated Circuit Computer Systems

MOBY — A Module Binder for the CMU-DA System

Knowledge-based Layout Tools: TALIB

Towards a Natural Language Interface for CAD

ULYSSES — An Environment for VLSI Design Automation

Exploitation of Low-Level Concurrency: An IMP

Compilation of Multiple Processor Interconnections

Polysilicon In Advanced Integrated Circuit Processes

On-Line Testable Processors and Testing of MOS VLSI Circuits

Clemson University

Electromigration in the Pulsed Mode

Charge Injection in Gate Oxides

Latent Electrostatic Discharge Effects

Colorado State University

Low Resistance Ohmic Contacts for VLSI Technology

Columbia University

VLSI Circuit Layout

Cornell University

One-Quarter Micron CMOS Device/Circuit Technology

High Density Memory Cell Considerations

Multilevel Integrated Circuits

Monolithic Optical Interconnect

Low Resistance Contacts

Reactive Ion Etching

Transmission Lines as Interconnects for VLSI

Ballistic Transport Devices

Laser Photochemistry for *In-Situ* Processing

"Post-Shrink" Periodic Submicron Device Structures

Heat Removal in ICs

Physics of Submicron Scale Electron Confinement

Noise Mechanisms in Small Devices

Electron Microscopy of Submicron Devices and ICs

Defects and Morphology of Interfaces

Polyimide Films for Interlevel Dielectrics

Damage Induced During Plasma Etching

Duke University (See *Microelectronics Center of NC)*

Florida, University of

The Optimization of Polysilicon Emitters for Bipolar Transistors

Georgia Institute of Technology

Investigations of Mechanical-Environmental Interactions in VLSI Bond Interfaces

A Computer-Aided Design Methodology for Analog LSI/VLSI

Illinois at Urbana/Champaign, University of

Investigation of Thermal and Accelerated Dopant/Surface Interactions During Vapor Phase Film Growth in VLSI Device Fabrication by MBE

Design Verification and Testing of VLSI Circuits

Design of Testable VLSI Circuits

Reliability Physics of Silicon VLSI Transistors

VLSI Arrays, Applications and Layout Techniques

Automatic Test Generation for Microprocessors

A Fault Simulator Using Multilevel Subscripted Ds

Built-In Self-Test for Microprocessors

Design of a Pipelined Floating-Point Multiplier with Recursive Fraction Unit

Reducing the Technological Cost of MOS Self-Checking Checkers

Fault-Tolerant Matrix Arithmetic and Signal Processing on Highly Concurrent Computing Structures

Design Rule Checker and Circuit Extractor

An MOS Fault Simulator with Waveform Information

A Multiple Instruction Stream Shared Pipeline Processor

Hierarchical Fault Simulation

Switch-Level Fault Simulation

Timing Verification

Channel Routing Algorithms

General Routing of Multiterminal Nets

Network Partitioning

VLSI Computing Arrays

Global Layout Techniques

Iowa, University of

Development of a Design Automation System for Speed-Independent Circuits

The Johns Hopkins University

Sources for Cluster Ion Beam Deposition

Massachusetts Institute of Technology

Surface-Energy-Driven Secondary Grain Growth for Si Epitaxy

Low Temperature Silicon Epitaxy by Low Pressure Plasma Enhanced CVD

Laser Induced Chemical Vapor Deposition of Active and Passive Materials

Plasma Assisted CVD of Refractory Metals and Silicides

Characterization and Modeling of the Plasma Etching of Polycide Structures

Controlled Heat Transfer for High Quality Liquid-Phase Recrystallization

Study of Stacked Device IC Technology

Ultra-Thin Gate Dielectrics for Scaled CMOS Technology

Zero Shrinkage Ceramic Tape for IC Packages

Michigan, University of

Sensors and Advanced Instrumentation For Equipment Diagnostics, Process Control, Wafer Diagnostics, and Process Evaluation

Modeling and Control of Semiconductor Facilities

End-Process Testing for Detection of Manufacturing Defects

Modeling of RIE Process for Characterization and Control

Application of Machine Vision and Logical Inspection Units to Manufacturing Process Control

Expert Systems for VLSI Manufacturing

Microelectronics Center of North Carolina [MCNC] *(including work performed by Duke University [DU], North Carolina State University [NCSU], The University of North Carolina at Chapel Hill [UNC/CH], and Research Triangle Institute [RTI])*

Ultra-Compaction Techniques for VLSI Layouts *[DU, MCNC]*

Shallow Junction Formation, Defects, and Structural Stresses *[DU, MCNC, NCSU, UNC/CH]*

Extrinsic Gettering of Impurities in Silicon Via the Introduction of Misfit Dislocations *[NCSU]*

Effects of Plasma-Enhanced Etching Processes and Cleaning on Surface Layer Damage and Contamination *[NCSU, UNC/CH]*

Plasma-Assisted Low Temperature Oxidation. Film Formation and Epitaxy *[MCNC, NCSU]*

The Role of Particles in Yield Considerations [RTI]

CMOS Latchup Modeling As Related to Process Limits *[DU, NCSU]*

Integration of Low Temperature Processing Into One Micrometer CMOS Technology *[MCNC, NCSU]*

Minnesota, University of

Three-Dimensional Integrated Circuits

Very Low Temperature Silicon Epitaxy by Sputtering

Application of Acoustic Microscopy to the Examination of ICs

Mississippi State University

Multilevel Interconnect Materials

Reactive Ion Beam Sources for VLSI

North Carolina at Chapel Hill, University of *(See also Microelectronics Center of NC)*

Transfer of Software Methodology to VLSI Design

Performance and Failure Analysis of Microelectronics Devices by Digital Scanning Electron Microscopy

North Carolina State University *(see Microelectronics Center of NC)*

Notre Dame, University of

Optimization of Incoherent Light and CW Laser Annealing in Si

The Pennsylvania State University

Thermal Nitridation of Silicon

Plasma and Reactive-Ion Etching With Fluorine Based Compounds

Purdue University

Advanced Models for Heterostructure Devices, including High-Speed Bipolar Transistors

Rensselaer Polytechnic Institute

Proximity Correction for E-Beam Patterning

Electron Beam Annealing

Ion-Cluster Beam Deposition

Mass Spectroscopy Analysis of Ion Cluster Beams

Resist Development for Ion, X-Ray, E-Beam and UV Lithography

Focused Ion Beam Processing

Liquid Metal Ion Sources for FIB

Research Triangle Institute (See *Microelectronics Center of NC)*

Rochester, University of

CAD Techniques for VLSI Layouts

South Carolina, University of

VLSI Digital Signal Processors

Southern California, University of

Laser Repair of Transparent VLSI Mask Microfaults

Stanford University

Performance Enhancement of VLSI Through the Use of Advanced Cooling Techniques

Technology of Multilevel Interconnections and Contacts for Submicron VLSI

Complementary MESFET Devices for VLSI Technology

Studies of the Origin of Silicon-Silicon Dioxide Interface States

High-Level Language for Representation of VLSI Fabrication Processes (FABLE)

Process and Equipment Modeling and Simulation

Generic Models for Semiconductor Fabrication Equipment

Specialized Test Patterns

A Hierearchical Parameter Distribution Control System: From Equipment to Process Circuit

Heterojunction Field-Effect Transistor Modeling and Development

The Texas A&M University

A Computer-Aided Design Methodology for Analog LSI/VLSI

Vermont, University of

MOS VLSI at Low Temperatures

Wisconsin, University of

Studies of Silicide Metallizations for VLSI

Yale University

Process-Induced Radiation Effects In Small-Dimension MOS Devices

Thin Insulators and Their Interfaces in Metal/Insulator/Semiconductor Systems

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*Returned to company August 1, 1984.

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