2005 ANNUAL REPORT

INDISPENSABLE

COLLABORATION

SRC®

SEMICONDUCTOR RESEARCH CORPORATION

"The semiconductor industry landscape is constantly changing. We've stayed ahead by leveraging SRC's expertise in managing university research directed toward meeting industry's needs. This has proved to be indispensable."

Wilbert van den Hoek, President and CEO, Novellus Development Corporation and SRC Board Member

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Overall SRC Snapshot of 2005

- 3,027 Technical Documents

- 1463 Students

- 16 New Patents

- 121 Contracts Launched in 2005

- 789 Liaisons

- 3,038 Event Attendees

- 147 New Tasks

- 51 Inventor Awards

In 2005, SRC continued its tradition of identifying and responding to emerging research needs of its member companies. For example, as the limits for the scaling of charge-based devices come more clearly into view, the industry has launched, through a new SRC subsidiary, the Nanoelectronics Research Corporation (NERC), the Nanoelectronics Research Initiative (NRI) to discover scalable information technologies beyond the limits of charge-based devices. The progress by NERC in 2005 has been nothing short of remarkable; launching six cooperative projects with existing National Science Foundation Centers and creating two new research centers with strong cooperation from industry and state governments. Plans for a third center in 2006 are on course. The overarching goal of NERC is to identify new technologies that can continue to offer to society the exponential gains in performance per unit cost that have been provided by CMOS for the past three decades and that will probably continue for CMOS for the next one to two decades. In particular, NERC seeks to demonstrate novel information processing devices with critical dimensions below 10 nanometers, to exercise them in simple computer circuits, and to demonstrate the potential for scaling these technologies to continue Moore's Law benefits beyond CMOS. This is a bold quest and will undoubtedly carry us to new frontiers of human knowledge.

In parallel with this new initiative, the Core Research Program and the MARCO Focus Center Research Program have continued to provide a large array of significant research results across the entire spectrum of semiconductor technologies. The combination of these two programs embraces research that ranges across the ITRS nodes from near development to the end of charge-based scaling. Later in this report, we provide examples of the research emerging from this comprehensive program in the research section. The structure of the section is in accordance with industry feedback on high priority areas for university-based semiconductor research. The relevance and rate of progress, as obtained from industry feedback, has never been higher.

An equally important product of SRC research is the generation of highly talented graduates who make a long-term impact on the competitiveness of SRC member companies. SRC programs support nearly 1,000 graduate students, each of whom is involved in highly relevant research. We are seeing an increasing demand for these students from our members and are doing all that we can to make them accessible to our members.

SRC's seventh TECHCON was held in Portland, Oregon in October 2005. This is the premier showcase where SRC students nearing the completion of their graduate programs give presentations and posters of their work to industry attendees. The event drew 442 participants including 158 student presenters. More details can be found on page 25.

> "The relevance and rate of SRC progress, as obtained from industry feedback, has never been higher"

In responding to various research needs of SRC member companies, it has become necessary to form subsidiary organizations, each established to meet the management style desired by our members, the technical goals and objectives, as well as defining and implementing government leverage and involvement. One ramification of this "multi-mode" organizational approach is that it became essential to be able to communicate to the stakeholders of each organization, as well as to the public, a clear set of messages that describe and characterize the subsidiary. At the same time, these subsidiaries need to be viewed as SRC companies to strengthen and maintain SRC's identity. An Ad-Hoc committee of the SRC Board of Directors is working through the definition of all SRC brands, including a new name for the SRC Core Research Program.

In conclusion, 2005 was a banner year for SRC with many opportunities to contribute to the technology infrastructure of our member companies and with new and exciting challenges. We at SRC are excited about our future opportunities to serve our member companies, the university community, our co-sponsors, and society at large.

Research Results
Relevantly Educated Talent
Integrated University Research Capability
Networking

VALUE

Circuit and system design
Design verification
Test and testability
Materials and processes
Packaging and
   interconnect
Advanced patterning
Mixed signal/analog
   technologies
Metrology
Environment, safety
   and health
Advanced device
   modeling and
   simulation

Over the past 23 years SRC member companies have invested $685M in cutting-edge semiconductor research supporting over 5,300 students and 1,110 faculty members at 196 universities worldwide. The marketplace and the complexion of the industry continue to change rapidly, presenting ever-greater global challenges to maintain critical research and to maintain SRC's reputation as a preferred sponsor of university research. SRC has continued aggressive efforts in executing and advancing its comprehensive Value Proposition. SRC's Value Proposition emphasizes all four dimensions of value: Creation, Delivery, Extraction, and Advocacy/Enhancement.

Creation

Member company representatives comprise 15 Technical Advisory Boards (TAB), which develop research needs statements, evaluate, and select programs proposed by the university community. A full spectrum of semiconductor technologies were investigated by the 487 research tasks funded during 2005 at 107 world-wide universities. Each task is reviewed during an annual research review attended by TAB members, university faculty, and SRC-funded students.

SRC funded 15 high-risk tasks under its Cross-Disciplinary Semiconductor Research (CSR) program. The goal of the CSR program is to foster exploratory, multi-disciplinary, high-risk university research leading to novel high-payoff solutions for the technology challenges faced by the semiconductor industry at and beyond the time horizons of the SIA International Technology Roadmap for Semiconductors (ITRS).

The SRC's seventh technical conference, TECH-CON 2005, held in Portland, Oregon in October, provided a forum for reviewing a major portion of the SRC research portfolio and for networking among industry, faculty, and students in TechFair and CareerConnections. All attendees were inspired by a special session on Biologically Inspired Silicon, chaired by Portland State University and SRC Principal Investigator Dan Hammerstrom. More information about TECHCON 2005 can be found on page 25.

In order to deliver relevantly-educated talent, SRC continued to enhance student programs as nearly 1,000 students participated in SRC-funded research in 2005. Of the SRC students graduating this year, 66% either went to work for SRC member organizations or are undergraduate or masters' students continuing to advanced degrees. Read more about SRC's student programs on page 24.

During 2005, SRC funded research with outstanding researchers at 107 universities including 26 institutions outside the United States. Professor Kaushik Roy of Purdue University and his team of 11 student researchers were awarded the SRC Technical Excellence Award for their investigations in the various aspects of device/circuit and architecture design for ultra low power digital sub-threshold operations. Dr. David Allstot of the University of Washington was recognized with the Aristotle Award for his outstanding contribution in the area of teaching, mentoring, and influencing a generation of circuit designers.

In 2005, SRC added 14 patents to its intellectual property portfolio (which currently includes 247 SRC-issued patents), further cementing the value of royalty-free licenses of research results, to which SRC members had early access. During TECHCON 2005, Sixty four Inventor Recognition Awards were presented.   Read more about intellectual property on page 28.

Delivery

In order to facilitate delivery of research results to member company engineers, SRC hosted 19 Technology Transfer e-Workshops. These real-time lectures and interactions with professors provide time-advantaged connections to university research by all member companies. The Internet-based meetings and the audio are archived for convenient referral on the SRC web site.

In addition, during 2005, SRC sponsored several workshops and special meetings including:

* MFD Meets DFM Forum
* Directed Self-Assembly of Materials for Patterning Workshop
* Sixth International Workshop on Future Information Processing Technologies (6th IWFIPT)
* CWG2 Nanoscale Characterization and Metrology Workshop
* Silicon Nanoelectronics and Beyond III Workshop (SNB)
* Workshop on Student Hirability

The SRC web site continues to be the "go to" place for all information related to SRC. A new feature added during 2005 was the "My Company" site. This custom-designed site is based upon the user's member company affiliation, providing targeted information for each individual. The electronic document library houses more than 16,000 publications, including nearly 2,200 new titles added this year.

Extraction

In order to assist the members with maximizing the value from SRC, we continually collect and share benchmark practices via the Benchmark Practice Handbook on the SRC web site. Participation metrics are also provided quarterly in order to help member company representatives monitor participation in key activities.

Approximately 300 member representatives participated in various advisory board meetings to set research budgets and research agendas, to both select and review research programs, and to meet with professors and students.

Nearly 790 Industrial Liaisons - voluntary member company engineers - participated in the Industrial Liaison program this year. They interface with the university researchers in order to help provide insight to industry issues, transfer technology back to their member companies, offer industry support, and provide mentoring to help prepare students for rewarding careers in the industry.

SRC also provides opportunities for member companies to participate directly in the management of the consortium process through the Industrial Assignee program. Six full-time assignees assist in managing the SRC research portfolio, as well as providing real-time access to the latest developments for their respective companies.

Advocacy/Enhancment

The Executive Technical Advisory Board representatives annually review the research output, and in 2005, they individually identified more than 150 "nuggets" of compelling research, which had or will provide significant contributions to our members' business, technology and/or product successes. Our member companies continued to enjoy net "ROI" of much greater than 250%. This was reflected in our annual member satisfaction survey score of 4.5 on a scale of 5.0.

Impact of SRC-guided Research

The 20 papers below, all written by SRC researchers, have each been cited more than 100 times. Papers cited as often as these are rare in scientific literature, and a few approach or exceed the number of citations given to papers of Nobel Laureates.

1. "High-κ Gate Dielectrics: Current Status and Materials Properties Considerations", by Wilk, Wallace, and Anthony (2001) UNT and USF

1072 citations, 330 citations by industry (31%)

2. "Nanotube Molecular Wires as Chemical Sensors", by Dai et al. (2000) Stanford

839 citations, 88 citations by industry (10%)

3. "Graph-based Algorithms for Boolean Function Manipulation", by Bryant (1986) CMU

822 citations, 197 citations by industry (24%)

4. "Point Defects and Dopant Diffusion in Silicon", by Plummer et al. (1989) Stanford

603 citations, 214 citations by industry (35%)

5. "Asymptotic Waveform Evaluation for Timing Analysis", by Pillage and Rohrer (1990) UT/Austin

314 citations, 112 citations by industry (36%)

6. "Alternative Dielectrics to Silicon Dioxide For Memory- and Logic Devices", by Kingon et al. (2000) NCSU

275 citations, 68 citations by industry (25%)

7. "Switching Devices Based on Interlocked Molecules", by Heath et al. (2001) UCLA

236 citations, 8 citations by industry (3%)

8. "Large-Scale CVD Synthesis of Single-Walled Carbon-Nanotubes", by Dai et al. (1999) Stanford

231 citations, 26 citations by industry (11%)

9. "The Gaseous Electronics Conference Radiofrequency Reference Cell – A Defined Parallel-Plate Radiofrequency System for Experimental and Theoretical Studies of Plasma-Processing Discharges", by Kushner et al. (1994) U Illinois/Urbana

202 citations, 33 citations by industry (16%)

10. "Molecular Random Access Memory Cell", by Reed et al (2001) Yale

193 citations, 28 citations by industry (15%)

11. "Reversible Electromechanical Characteristics of Carbon Nanotubes Under Local-Probe Manipulation", by Dai et al. (2000) Stanford

171 citations, 18 citations by industry (27%)

12. "Ferroelectric Materials for 64 Mb and 256 Mb DRAM", by Parker and Tasch (1990) UT/Austin

169 citations, 46 citations by industry (27%)

13. "Hole Injection SiO_2 Breakdown Model For Very Low Voltage Lifetime Extrapolation", by Schuegraff and Hu (1994) Berkeley

163 citations, 65 citations by industry (40%)

14. "2-Dimensional Modeling of High Plasma-Density Inductively Coupled Sources for Materials Processing", by Ventzek et al. (1994) U Illinois/Urbana

162 citations, 36 citations by industry (22%)

15. "The Dielectric Response as a Function of Temperature and Film Thickness of Fiber-textured $(Ba,Sr)TiO_3$ Thin Films Grown by Chemical Vapor Deposition", by Kingon et al. (1997) NCSU

143 citations, 39 citations by industry (27%)

16. "BSIM - Berkeley Short-Channel IGFET Model for MOSTransistors", by Sheu et al. (1987) Berkeley

131 citations, 43 citations by industry (33%)

17. "Plasma-Enhanced Chemical Vapor-Deposition –Differences Between Direct and Remote Plasma Excitations", by Lucovsky and Tsu (1987) NCSU

128 citations, 13 citations by industry (10%)

18. "Threshold Voltage Model for Deep-Submicrometer MOSFETs", by Hu et al. (1993) Berkeley

118 citations, 42 citations by industry (36%)

19. "Numerical Investigation of the Kinetics and Chemistry of RF Glow-discharge Plasmas Sustained in He, N_2, O_2, $He/N_2/O_2$, $He/CF_4/O_2$, and SiH_4/NH_3 Using a Monte-Carlo-Fluid Hybrid Model", by Sommerer and Kushner (1992) U Illinois/Urbana

115 citations, 16 citations by industry (14%)

20. "Importance of Space-Charge Effects in Resonant Tunneling Devices", Lundstrom et al. (1987) Purdue

103 citations, 17 citations by industry (17%)

Companies Participating in the NRI

Advanced Micro Devices, Inc.
Freescale Semiconductor, Inc.
IBM Corporation
Intel Corporation
MICRON Technology, Inc.
Texas Instruments, Inc.

As the ultimate limits to the scaling of CMOS (Complementary Metal Oxide Semiconductor) technology are getting closer, new approaches in emerging areas in electronics at the nanoscale need to be explored. The Nanoelectronics Research Initiative (NRI) is a program supported by the above six member companies of the Semiconductor Industry Association (SIA), who directed SRC to establish the Nanoelectronics Research Corporation (NERC), a wholly-owned SRC subsidiary, to develop and administer a university-based program to address this vital issue. The goal is to demonstrate novel computing devices with critical dimensions below 10 nanometers and to exercise them in simple computer circuits so that industry can extend Moore's Law far beyond the limits of CMOS.

The key objectives for this first year were to establish NERC as a high visibility player in the field of nanoelectronics and to start building not only the organization, but to lay the foundations for a successful scientific program.

In response, NERC joined forces with the National Science Foundation and solicited proposals from existing NSF nanoscience centers for supplemental funding of NRI-related activities at these centers. Six centers were selected and are jointly funded by NSF and NRI. Industrial liaison committees with participants from the NRI companies are working closely with the center directors to provide input on the industry's needs and to provide feedback as appropriate.

In addition, NERC solicited proposals from all U.S. institutions qualified to do research in areas based on computational state variables other than electronic charge, non-equilibrium systems, or novel energy transfer mechanisms. Collateral technology critical to beyond-CMOS information processing, such as interconnects, memories, nanoscale characterization, thermal management, and directed self assembly, were also considered. Efforts were selected that comprise in a unique fashion a number of universities exploring a variety of potential alternatives. Two new research centers are currently being formed:

- The Western Institute of Nanoelectronics (WIN) in California is headquartered at the UCLA Henry Samueli School of Engineering and Applied Science. WIN participants are from three University of California (UC) campuses (Los Angeles, Berkeley, and Santa Barbara) and Stanford University. WIN will focus on novel spintronics and plasmonic devices. In addition to NRI funding, this center will receive additional direct support from Intel and the UC Discovery program.

- The Institute for Nanolectronics Discovery and Exploration (INDEX) in Albany, New York, is headquartered at the College of Nanoscale Science and Engineering of the State University of New York-Albany (SUNY-Albany). It will also include the Georgia Institute of Technology, Harvard University, the Massachusetts Institute of Technology, Purdue University, Rensselaer Polytechnic Institute, and Yale University. INDEX will focus on the development of nanomaterial systems, atomic-scale fabrication technologies, predictive modeling protocols for devices, subsystems and systems, power dissipation management designs, and realistic architectural integration schemes for realizing novel magnetic and molecular quantum devices. INDEX will receive additional direct funding from IBM, and support from New York State is expected.

In addition, NERC announced an individual grant for exploratory work in spintronics to the research team led by Professor Banerjee at the Univ. of Texas/Austin.

The Microelectronics Advanced Research Corporation (MARCO), jointly supported by DARPA, funds and operates five university-based research centers in microelectronics technology. Its charter initiative, the Focus Center Research Program (FCRP), is designed to expand pre-competitive, cooperative, long-range applied microelectronics research at U.S. universities in those technical areas that are critical to maintaining industry growth in the United States.

GSRC

The Univ. of California/Berkeley is the lead university for the Gigascale Systems Research Center (GSRC), with Professor Jan Rabaey as the Center's Director. The Center's research agenda focuses on pertinent problems the semiconductor industry faces in the next decade in the areas of system design, integration, test, and verification. To sustain current growth, the industry requires orders of magnitude of improvement in energy efficiency, cost, reliability, and time-to-market.

To address the multiple challenges within this focus, the Center is structured along nine interlocking research themes, each led by a theme leader. The horizontal themes, Heterogeneous System Design & Integration and Soft Systems, represent two visions on how integrated systems are to be realized. A new horizontal theme, Microarchitecture, has been initiated jointly with the C2S2 Focus Center. These horizontal themes are combined with four vertical ones, each of which addresses one particular aspect of embedded integrated system design. The Power-Aware Systems, Reliable Systems, System Verification, and Embedded Self-Test themes, respectively, address the power and energy, reliability, verification, and test roadblocks that are looming on the horizon. Finally, the System-Level Living Roadmap provides an environment to explore how the different cost metrics of design will evolve in the next decade, taking a system-level view. This high-level perspective is unique and complements as well as builds on top of the existing roadmapping efforts. These efforts, which encompass and integrate all the research activities of the Center, are essential in identifying emerging challenges and in steering the research evolution of the Center.

C$_2$S$_2$

The Focus Center for Circuits and Systems Solutions (C2S2) is led by Carnegie Mellon University. Professor Rob Rutenbar is the director. The Center aims to develop new circuit design techniques needed to convert novel devices into robust performance across the most diverse range of applications.

Relentless scaling of semiconductor devices toward fundamental physical limits threatens to make obsolete today's most basic circuit design assumptions. Today's landscape of familiar trade-offs (area, speed, power, frequency, noise, reliability, linearity, yield, and cost) is shifting radically. To build tomorrow's complex, integrated, heterogeneous systems, the industry requires a foundation of circuit designs it can trust.

Circuits play a unique role in the "food chain" from materials to gigahertz. They hide the physics from designers; they form the most basic system-building blocks; and they provide the essential traction for handling billions of competing system implementation details.

C2S2 research invents the new design techniques necessary to convert near-limit scaled devices and post-silicon devices into useful system-building blocks. It targets these design innovations across diverse design domains—digital, analog, RF, photonic, and MEMS designs.

Research in the Circuit Design Center provides the needed link between devices and system design.

IFC

The Interconnect Focus Center (IFC) is led by the Georgia Institute of Technology. Professor James Meindl is the director. The Center conducts research to discover and invent new electrical, optical, and thermal interconnect solutions that will meet or exceed ITRS projections and enable hyper-integration of heterogeneous components for future terascale systems.

The Center focuses on research of all aspects of the wiring that connects the millions of transistors on a microchip, from process to system-level architecture. Today and in the future, the microelectronics and nanotechnology industries will lead the evolu-

tion of technology in industries from automotive to medical and from computing to aviation. IFC strives to stay atop all advances in these fields and play a major role in driving this technology into the future. To that end, the Center's research themes have evolved to accommodate this goal.

MSD

Materials and Devices research is conducted by the Center for Materials, Structures and Devices (MSD) at the Massachusetts Institute of Technology. Professor Dimitri Antoniadis is the Center Director. Its focus is to explore and determine the most promising path for microelectronics in the next two to three decades by pursuing two overlapping approaches: scaling of CMOS to its ultimate limit and interdisciplinary exploration of new-frontier devices.

Since its inception in 2000, the MSD Center has successfully launched entirely new material combinations for high performance CMOS applications while pushing new frontier devices, such as carbon nanotubes, to new heights of performance through the combination of novel chemical synthesis of nanostructures with advanced front-end processes borrowed from silicon technology. In addition, the MSD Center is well along its way to establishing realistic benchmarking of highly disparate devices on equal footing via close collaboration of experimentalists from different disciplines with advanced modeling and simulation researchers.

Research in this Center is organized into five research themes. Four of the themes concentrate on experimental research in device technology while the fifth collaborates with the other four in addressing key process and device issues by advanced modeling and simulations.

FENA

Research in Nano Materials is conducted by the Focus Center on Functional Engineered Nano Architectonics (FENA), the newest Focus Center. Professor Kang Wang of UCLA is the Center Director. The Center's research is directed at resolving the cross-cutting materials and device challenges related to beyond-CMOS in order to create new information processing paradigms with greater capabilities.

In order to tackle major challenges common to all nanometer scale devices, new nanoscale materials and processes are needed to address the core problems of nanoscale technology. Opportunities exist for creating a new generation of nanoscale materials, structures, and devices, which will extend semiconductor technology to CMOS limits and beyond, and provide heterogeneous interfaces of new nanosystems, enabling a combination of molecular and biological functions that lead to new paradigms of information processing and sensing. Through this new generation of nanostructured materials, the semiconductor industry will continue to expand and create new applications of monolithically integrated (CMOS, molecular, and biomolecular) nanosystems. FENA focuses on the materials challenges at the nanoscale for fulfilling these opportunities.

MARCO Snapshot of 2005

- 821 Technical Documents

- 543 Students

- 60 Invention Disclosures

- 30 Inventor Awards

- 2,150 Event Attendees

The Core Research Program at SRC has operated continuously since 1982. It is characterized by:

- Strong industry involvement in planning, selecting, evaluating, and operating research projects
- International membership and research program execution
- Well-developed technology transfer processes
- Emphasis on student degree program success
- Research horizons centered at 22 nm, bridging to development and intersecting MARCO programs
- Primarily, but not exclusively, oriented toward individual investigator projects
- Committed to a focus on silicon technology research
- Active management and professional leadership by a talented staff

In 2005, a total of 487 research tasks were conducted in the Core Research Program in the five Science Areas and the Cross-Disciplinary Semiconductor Research Program. There were 443 faculty involved in the Core Research Program at 107 universities, and 970 students participated in the research. The Science Areas are each supported by an industry Science Area Coordinating Committee (SACC) and each Science Area executes its programs through a set of topical thrusts. An industry Thrust Advisory Board (TAB) supports the programs in each of the thrusts. Oversight for the industry advisory structure is provided by the Executive Technical Advisory Board (ETAB). In total, 307 industry specialists served as SACC and TAB members. Industry involvement is further strengthened by the Industrial Liaison Program whereby industry people serve as 'friends of the research' to provide further support for the research projects. There were 789 individuals serving as industrial liaisons.

The specific structure of the SRC Core Research Program is:

Computer-Aided Design and Test Sciences (CADTS)
- Verification
- Test and Testability
- Logic and Physical Design

Device Sciences (DS)
- Digital CMOS
- Analog and Mixed Signal
- Memory Technologies
- Modeling and Simulation
- Compact Modeling

Integrated Circuit and Systems Sciences (ICSS)
- Circuit Design
- Integrated System Design

Interconnect and Packaging Sciences (IPS)
- Back-End Processes
- Packaging

Nanomanufacturing Sciences (NMS)
- Factory Systems
- Patterning
- Environmental Science and Health

Cross-Disciplinary Semiconductor Research Program (CSR)

SRC Snapshot of 2005

- 2,206 Technical Documents

- 970 Students

- 14 New Patents

- 21 Inventor Awards

- 121 Contracts Lanched in 2005

- 789 Liaisons

- 147 New Tasks

- 3,038 Event Attendees

The partnership that SRC embodies between universities and industry has proven to be a powerful force for innovation and progress. In the following paragraphs, we give a brief sample of the many research results that emerged from the comprehensive SRC research program including results from the MARCO Focus Center Research Program (FCRP) and the Core Research Program. We gratefully acknowledge the support and contributions of our government partners in this research enterprise including DARPA, NSF, and the State of New York.

The SRC's overarching goal is to conduct university research that sustains the unprecedented rate of progress in integrated semiconductor technologies that has had such a transforming impact on society for approximately four decades. From our vantage point, we believe that even greater achievements lie ahead. Research in semiconductor technology is both challenging and exciting because it takes us into domains of endeavor that expand our understanding of the material world, and it astounds us with complexities and capabilities of an order that have not heretofore been experienced by humankind. The recognized driver for the exponential gains in performance per unit cost is feature-size scaling of the ubiquitous MOSFET device. While this is correct, it is only part of the story. The manufacturing and design infrastructure to cost-effectively produce integrated circuits has undergone continuous and, in many cases, radical changes in order to support feature-size scaling. As industry begins to move to the 45 nm node and beyond, a myriad of technological challenges must be overcome to achieve ultimately scaled CMOS. In response, SRC conducts a broad spectrum of research to address challenges in all aspects of semiconductor technology. In what follows, we briefly describe a few of the many salient accomplishments by SRC research in 2005. (The following superscript annotations have been used at the end of appropriate paragraphs to indicate MARCO research through the FCRPs: C2S2[1,] FENA[2], GSRC[3], IFC[4], MFD[5]).

CMOS Structures, Materials and Processes

SRC's research on MOSFETs can be comprehended from Figure 1 in the areas: a) high-κ and low-leakage dielectrics (Region 1/Figure 1), b) metal gate electrodes (Region 2/Figure 1), c) partially or fully depleted high-mobility, high-carrier-velocity channels with low channel leakage (Region 3/Figure 1), and d) low-leakage ultra-shallow source/drain junctions and contacts (Region 4/Figure 1). Arrows I_{GL}, I_{CL}, and I_{SL} depict various current leakage paths that must be minimized to lower static power dissipation: I_{SL} is drain-substrate or the band-to-band drain tunneling current, I_{GL} is gate dielectric leakage current, and I_{CL} is the thermionic channel leakage current.
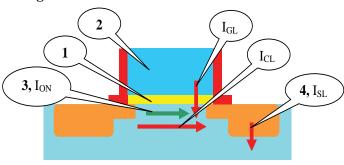

Figure 1. Schematic MOSFET structure illustrating device research topics

SRC's device research program is aimed at increasing the channel "on-current" (I_{on}) while maintaining or decreasing the "off-current" ($I_{off} = I_{GL} + I_{CL} + I_{SL}$). Scaling the MOSFET size to ever smaller dimensions to increase I_{on} and transistor speed exacerbate these leakage mechanisms exponentially increasing their impact on the device power dissipation and performance. SRC's device research accomplishments in 2005 directly address these MOSFET performance needs and requirements.

The Front End Process Transition Center is focused on two primary areas: (a) developing high-κ dielectrics to achieve 0.5 nm Equivalent Oxide Thickness (EOT) and (b) the associated metal gate electrodes, where the high-κ and metal gate issues are considered together rather than as separate topics. Channel strain leading to enhanced carrier mobility, velocity and, thereby higher I_{on} and transistor speed, is the focus of several modeling and simulation as well as electrical and physical characterization research efforts. Use of strain (tensile and compressive) in the channel of both n- and p-MOSFETs, respectively, is providing CMOS technology a substantial boost (up to +30%) in the all-important transistor on-current, I_{on}. Research on $Si_xGe_{(1-x)}$ source/drain stressors [Ozturk, North Carolina State University (NCSU)] is determining what level

of boron concentration is required for optimal performance with a given Ge alloy composition and $Si_xGe_{(1-x)}$ source/drain thickness. At the Univ. of Florida, the first explanation of the electric-field dependent hole mobility in compressively strained p-channel MOSFETs was recently provided. They also explained that the smaller threshold voltage shift for NMOS MOSFETs for uniaxial process strain is due to less bandgap narrowing and the strained gate [Thompson, Univ. of Florida].

Hoyt's group [Mass. Institute of Technology (MIT)] has fabricated and analyzed MOSFETs in new nano-engineered materials, specifically (a) *ultra-thin* Strained Silicon Directly on Insulator (SSDOI), and (b) *ultra-thin channel* Strained Si/Strained SiGe/Strained Si Heterostructure On Insulator (HOI). Enhancements in electron mobility (up to 1.8x) and hole mobility (up to 3x) were measured compared to conventional silicon-on-insulator devices, even for ultra-thin channel layers[5].

An important issue with application of high-κ gate dielectrics (Region 2/Figure 1) onto Si is the need to minimize the SiO_x interfacial oxide between the high-κ gate dielectric and the Si channel (Region 3/Figure 1). Research on new gate metal electrodes (Region 1/Figure 1) recently has shown that use of a reactive metal gate can essentially eliminate this interfacial oxide through an oxygen scavenging process [McIntyre, Stanford University].

Exploring new electronic device structures for the longer time horizon beyond highly scaled CMOS, the Kaloyeros group [Univ. of Albany], in their continued investigation of substrate-directed self-assembly of polypeptide-based molecular device structures, has centered recently on controlling precise placement of molecular groups for molecular device applications. The left panel of Figure 2 shows experimental Scanning Tunnel Microscopy (STM) data of polypeptide materials which have undergone substrate-directed assembly on atomically smooth graphite. The right panel of Figure 2 shows a schematic of the orientation of the peptide based on molecular modeling. The yellow arrows denote the direction for charge transfer along the polypeptide beta-turn moieties or parts of a molecule. The ability to precisely control the direction and density of polypeptide packing is being developed to enable controllable electron transport via

a Si-back-gate, Molecular Field Effect Transistor (MFET) geometry[5].
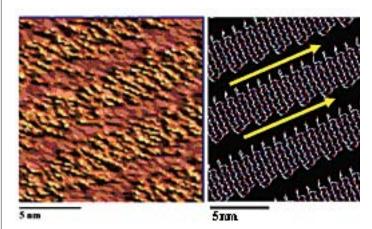

5 nm   5 nm

Figure 2. Polypeptide materials which have undergone substrate-directed assembly on atomically smooth graphite (left). Schematic of the orientation of the peptide based on molecular modeling (right)

Interconnect Technologies

Researchers at Georgia Institute of Technology (GIT) have addressed the challenge of identifying the capabilities available with extensions of existing copper low-κ technology. Their approach has been to study the impact of size effects including both surface scattering and grain boundary scattering on the design and performance of multi-level interconnect networks, using an n-tier methodology. A complete application of this methodology shows that moderate changes in wiring pitches and the number of metal levels (±40% and 10%, respectively) can address more than 4x increases in resistivity of minimum sized wires. This conclusion gives credence to the belief that traditional copper low-κ technology can continue to meet the needs of Moore's Law for, at least, the next decade [Meindl/Naeemi, GIT].

The Meindl/Naeemi group has also addressed the comparison of conductivity between minimum geometry Cu wires and carbon nanotubes. Their work shows clearly that carbon nanotube bundles can provide greater than 100% better conductivity than offered by minimum geometry Cu wires[4.]

Metrology to comprehend the results of advanced processing is a critical requirement. Researchers at Cornell University have provided a major advance in capabilities to visualize extremely small

volumes in a tomographic approach using imaging data from Tunneling Electron Microscope (TEM) and Scanning Tunneling Electron Microscope (STEM). Figure 3a shows a reconstructed image of a Cu via structure with a stress void area. Figure 3b is a close-up 3D reconstruction of the stress void. The imaged component has a volume of only $(210 \text{ nm})^3$. This small volume can be rotated in three dimensions to view ridges and facets to assist in process development, reliability analysis, and other critical tasks [Muller, Cornell University].
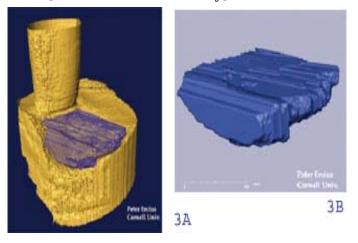

Figure 3. A Cu via structure with a stress void highlighted in blue (3A). An expanded view of the void by itself. (3B)

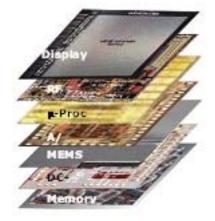Cost, performance, and portability drive the push for increased system integration on a single chip, e.g., the coexistence of analog and digital systems on the same chip to comprise a mixed-signal system. Mixed-signal design is plagued by parasitic interactions induced by switching digital circuits, which can adversely affect the performance of the analog subsystem through noise propagation in the shared substrate. Using a novel 3D field solver, Reif's group at MIT has shown that as much as 85 dB of isolation can be realized between 3D die levels at 5 GHz (Figure 4). This excellent isolation indi-

Figure 4. A 3D approach to mixed signal integration

cates the attractiveness of 3D Mixed Mode integration for mixed-signal systems.

At Stanford University, a major breakthrough has occurred in optical interconnects to silicon chips. They have found, in germanium quantum wells grown on silicon substrates by standard silicon growth techniques, the same strong electroabsorption mechanism (the Quantum-Confined Stark Effect (QCSE)) that allows high-performance optical modulators in III-V compound semiconductors. Indeed, this mechanism may actually be better in these group IV materials than it is in the III-Vs, and it is very promising for optical modulator devices that can meet the demanding metrics for dense optical interconnects (< 1 V, < 10 mW, > 10 GHz). Ongoing work is now attempting to demonstrate the first devices with this QCSE mechanism. They have shown that the QCSE mechanism can also be made to work across the wavelength region, which is most important for telecommunications – the "C-band" near 1.55 microns wavelength. A diagram of the diode structure is shown in Figure 5 [Harris/Miller group, Stanford University][4].
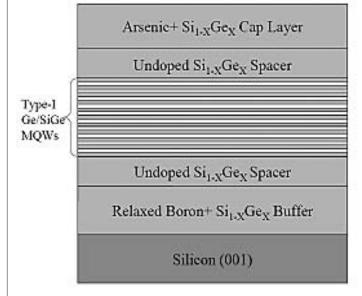

Figure 5. Diode structure for high performance optical interconnect applications

The use of pseudo-epitaxy via crystalline substrates has resulted in an ordered long-range (~100's of nm to μms) assembly of molecular wire arrays with pitches less than 5 nm. An example of such an

ordered array of ten parallel molecular wires is shown in the scanning tunneling micrograph (Figure 6). The pitch for the molecular wires is 4.7 nm and the wire to wire separation is less than 2 nm. Corresponding theoretical modeling has demonstrated material pathways to thermally-stable quantum channel formation in these materials[4].
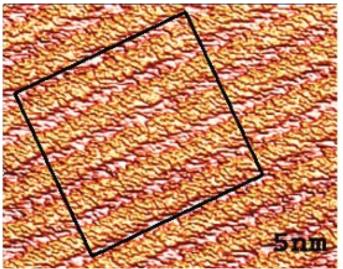

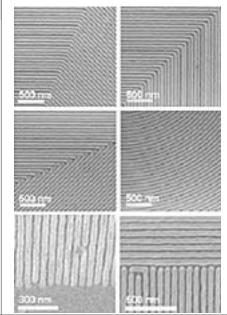Figure 6. Micrograph for a molecular wire assembly

An architecture for "Light-Wire" interconnects to integrate all optical components (laser, waveguide, isolator, and detector) on a silicon substrate was proposed. The IFC is currently investigating polymer based waveguides for low loss, high-speed data transmission, including; high performance Vertical Cavity Surface Emitting Laser (VCSEL), modulators for light generation and control, and high speed Ge based detectors for the total "Light Wire" system. This architecture is compatible with both intra-chip and inter-chip optical interconnects [Miller, Stanford University][4].

With decreasing dimensions, on-chip conductors, such as clock and power distribution networks, require accurate modeling of skin and proximity effects; and such modeling methods can be expensive in terms of the number of circuit elements. Though much previous work has focused on how to model skin effect efficiently by volume discretization, careful analysis has shown that skin effect can be ignored in many cases with small overall error, providing tremendous reductions in circuit complexity on the order of 10^6-10^8 over full 3D extraction, thereby greatly simplifying circuit simulation [Ismail, Northwestern University].

Novel intra-chip communications algorithms, protocols, and techniques using Network-on-Chip (NoC) architectures are also being developed which promise to overcome many of the problems associated with conventional interconnect such as congestion and latency. This research will accelerate IC developments involving design of on-chip multi-core interconnection. Simulations that are based on 130 nm and 70 nm technology parameters reveal up to 5.5x and 17x reduction in power and area, respectively, of serial vs. 32-bit multi-layer parallel link [Cidon, Technion Israel Inst. of Technology].

Patterning and Metrology

The following set of 2005 results reflects novel materials and assembly methods that are likely to enable extensions of CMOS fabrication technology to its ultimate limits.

At the Univ. of Wisconsin/Madison (UW/Madison), the Nealey/DePablo group report breakthrough results that demonstrate the feasibility of fabricating non-regular device-oriented nanostructures on substrates via the directed assembly of block copolymers. They direct ternary blends of diblock copolymers and homopolymers that naturally form periodic arrays to assemble into non-regular device oriented structures on chemically nanopatterned substrates. Redistribution of homopolymer-facilitated, defect-free assembly in locations where the dimensions of the domains deviated significantly from those formed in the bulk. The ability to pattern non-regular structures using self-assembling materials creates new opportunities for nanoscale manufacturing (Figure 7).

Figure 7. Self-assembled non-regular nano-structures

A table-top large core pulsed fiber laser system that produces Extreme Ultra-Violet (EUV) radiation at 13.5 nm has been developed, which demonstrated nanosecond multi-mJ energy pulses with high output beam quality, achieving greater than 10^{10}-W/cm^2 peak intensities on solid-Sn targets required for efficient EUV generation [Galvanauskas, Univ. of Michigan]. This set-up is scalable to multi-kW average powers and opens a promising pathway for production-worthy Next Generation EUV Lithography Tools.

A new strategy for investigating shot noise-induced Line-Edge Roughness (LER) by continuous model-based simulation, which applies a discrete model at the 1-2 nm scale for exposure, a continuous model at the 7 nm scale for Post-Exposure Bake (PEB), and a newly developed continuous Statistical Lateral Dissolution Model (SLDM) at 1 nm scale for development was reported. This efficient LER simulator has been used to investigate factors that impact LER generation, including non-Fickean diffusion, shot noise, and resist contrast. SLDM has also been applied to analyze Large Unlikely Roughness Event (LURE) that can lead to chip failure [Neureuther, Univ. of California/Berkeley (UCB)].

Researchers at Northwestern University have reported a novel characterization approach, Scanning Near-Field Ultrasound Holography [SNFUH], which could overcome the limitations of existing imaging systems. This approach, based on the holographic interference of a specimen's acoustic wave with that of a reference cantilever, allows for extraction of an acoustic wave's 'phase'; thereby revealing sub-surface nanoscale defects and features. They have provided proof-of-concept of SNFUH's ability to achieve sub-surface nanoscale non-destructive imaging (Figure 8) [Dravid/Shekhawat, Northwestern University].
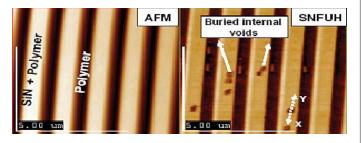

Figure 8. Scanning near-field ultrasound holography

A holographic aerial image-recording technique that can characterize both phase and amplitude information of coherent images was demonstrated by the Boker group [UCB - SRC/DARPA Lithography Network]. The technique can be applied to the microscopic characterization of isolated defects on EUV multi-layer mask blanks with full characterization of opaque and phase defects. The holographic method is of particular interest because few other methods exist that can quantify both the phase and the amplitude of submicrometer-sized defects on EUV mask blanks.

Results arising from improvements in long range dimensional control and reduced LER in features patterned via directed self-assembly versus conventional top-down lithography demonstrate the feasibility of tuning the lateral dimension of the final patterned feature by selecting appropriate dimensions of the polymeric blocks. This suggests a strategy for dimensionally tuning resists to smooth out and heal lithographically induced long range dimensional variability, offering reduced process noise. Additionally, the post-etch LER of dense line/space structures appears to be roughly half of that for lithographically patterned and etched PolyMethyl MethAcrylate (PMMA) [Nealey, UW/Madison].

Prof. Smith, at Rochester Institute of Technology (RIT), reports achieving 26 nm half pitch features using 193 nm [NA=1.85] evanescent imaging. These results suggest the possibility of addressing sub-32 nm lithography requirements with optical tools.

Thermal Management

Modern high-performance microprocessors and Digital Signal Processors (DSPs) are severely limited by thermal considerations. Microprocessors suffer from performance limitations in workstation applications, and both microprocessors and DSPs cannot be operated at full capacity in hand-held applications because of thermal limitations. These problems are becoming increasingly difficult with shrinking device geometries and increasing circuit complexity, and are being addressed by SRC.

By adding nanoscale materials to currently available Thermal Interface Materials (TIMs), major advantages to TIMs have been demonstrated. Specifically, they have shown that 1) the addition of nanotubes

and metallic nanoparticles to conventional TIMs can lead to greater than 2x increases in conductivity; 2) the conductivity of single carbon nanotubes is significantly reduced by lateral conduction in bundles of carbon nanotubes; and 3) vertical carbon nanotube arrays, as shown in Figure 9, can provide significantly increased thermal conductivity between chips and thermal heat spreaders, but the contact resistance at the nanotubes/spreader interface must be significantly reduced to take advantage of the nanotube conductivity [Goodson, Stanford University].
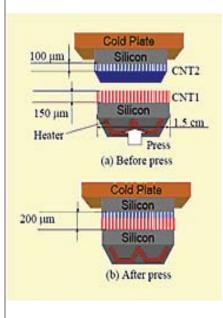

Figure 9. Vertical carbon nanotubes arrays used as TIM between silicon structures

Continuously increasing power consumption of microprocessors calls for liquid cooling. An on-chip microfluidic heat sink represents the highest integration level of the liquid cooling, which can remove ultra high heat flux ($\geq 790w/cm^2$), eliminate the thermal interfaces, and enable direct hot-spot cooling. In the past year, low-temperature CMOS compatible processes were developed for microchannel fabrication at the wafer back-side. Through-wafer fluidic paths and micro-pipe inlets/outlets were used as the thermal-fluidic I/Os to enable the on-chip microfluidic heat sinks with ultra-small form factor (Figure 10). Test chips with thin-film heater arrays have been fabricated. The resulting "microfluidic flip-chip" has been successfully bonded onto a Printed Wiring Board (PWB) substrate using conventional chip assembly processes and simultaneous electrical and fluidic interconnections were demonstrated. Theoretical analysis indicates that the ITRS projected power dissipation can be achieved at relatively low pressure and pumping power [Kohl, GIT][4].
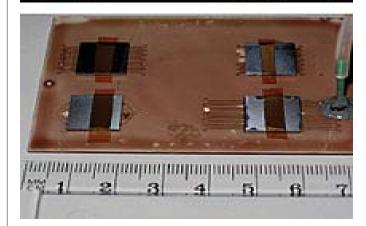

Figure 10. Micropipes and solder bumps (top) and an example of a test chip mounted on board with chip-board microfluidic connections (bottom)

Compiler support for parallelizing embedded applications on chip multiprocessors in a temperature sensitive manner has been investigated by the Hwu group at the Univ. of Illinois/Urbana-Champaign (UIUC). The approach optimizes power, temperature and performance within a unified framework, and experiments with a set of benchmarks show about 10% reduction in peak temperatures.[3]

Advanced Packaging

The need for ICs with very high numbers of signal input-outputs that will be used in SoC configurations in the coming years, as predicted in the ITRS, presents major problems for conventional packaging techniques. Our researchers have invented and demonstrated capacitively and inductively coupled interconnect systems that replace signal pin solder bumps, achieving 4,800 power/ground and 4,200 signal I/Os on an 18x18 mm chip (Figure 11). The novel technique maintains high performance, robust manufacturability, and demonstrates lower power

than conventional connectivity systems. Bit Error Rate (BER) measurements on both capacitively and inductively coupled systems obtained results better than 10^{-12} [Franzon, NCSU].

Figure 11. Technology for inductive/capacitive chip-to-package connection

At the Univ. of California/Los Angeles (UCLA), researchers have identified and modeled a significant new failure mechanism in Pb-free solders. Their results have shown a critical difference between solder balls attached to underbump metallization on chips and solder bumps attached to boards. The test setup and resulting defect growth are shown in Figure 12. The current density was 3.5×10^3 A/cm² in this experiment. The ambient temperature was 50°C. The susceptible bumps were found to be those where current entered into the flip chip solder bump from the upper left corner in the figure. This is the corner where the solder bump interfaces with the chip and current crowding occurs. This current crowding leads to a pancake-type void formation across the cathode contact, and finally, failure of the Pb-free solder joint [Tu, UCLA].

In related work, failure mechanisms at high-strain rates under overlapping stresses have been investigated. This is a particularly timely research topic as more and more hand held electronic items, which may be dropped frequently, are being used. This is an extremely complicated problem because there are so many different types of systems to consider, and the stresses are so varied. The approach taken by the Lall group [Auburn University] is to identify the leading indicators of damage progression prior to complete failure, and to develop a damage-equivalency methodology to correlate standard test conditions to widely varying designs and use conditions. Their work has led to a unique wavelet decomposition methodology for transient responses to stresses and correlating these to damage indicators. The long term results of this type of investigation will be extremely valuable to member companies dealing with hand-held electronics.

Factory Operations

In the area of process control, data and model requirements for fab-wide control have been developed and multi-step control algorithms are being tested [Qin, Univ. of Texas/Austin (UT/Austin)]. In addition, a Partial Least Squares (PLS) model, based on simulation and published survey analysis that provides information about various fab disruptions, has been developed. This model demonstrates through simulation the use of Self Organizing Maps (SOMs) and Bayesian Networks (BNs) for integration of in-situ sensing, equipment reliability, and maintenance and inspection data to predict semiconductor fabrication process yield.

In the area of supply chain, researchers have developed new models for short term forecasting for product families, using Support Vector Machines (SVMs) and commercial optimization software.
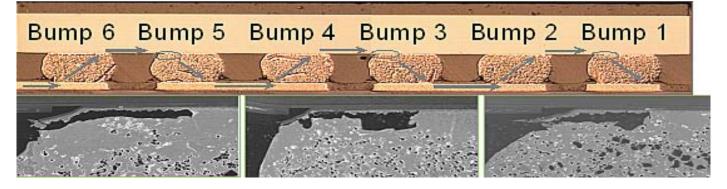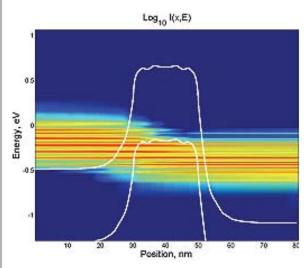

Figure 12. Reliability related failures in Pb-free solders caused by current crowding at susceptible corners

This tool is being piloted at one of the member companies [Raghavan, Indian Institute of Science]. A new demand characterization model that is based on leading indicators and lifecycle growth models has also been developed [Berger, Lehigh University]. Earlier results indicate that a sufficiently strong leading indicator typically can be found within a cluster of products with good correlation values and time lags appropriate for planning and that a leading indicator can be used to improve the demand scenarios generated by a group of lifecycle growth models.

TCAD

Three examples of modeling and simulation contributions made in 2005 are cited below. The first is a quantum transport simulation, (Figure 13), showing the energy-resolved current in a carbon nanotube n-MOSFET under high negative gate bias where band-to-band tunneling occurs. Electrons from the source tunnel into the forbidden gap in the channel, emit an optical phonon, fill a state in the valence band, and then tunnel through the bandgap into the conduction band of the drain. The I-V characteristics display a highly desirable sub-60mV/decade subthreshold swing, in agreement with recent experiments from IBM [Lundstrom, Purdue University].

Figure 13. Energy-resolved current in a carbon nanotube n-MOSFET under high negative gate bias

The Lundstrom group also has theoretically modeled ballistic transport for Si, Ge, GaAs, and InAs channels (Region 3/Figure 1). They found that a Ge channel offers the highest on current I_{on} for n- and

p-channel devices, whereas a low density-of-states degrades I_{on} for GaAs and InAs channel devices.

Other researchers have developed a novel approach to systematically generate models for Negative Bias Temperature Instability (NBTI) based on the diffusion distance of hydrogen at a given time and the density of hydrogen at the Si/SiO_2 interface [Roy, Purdue University]. This research focuses on experimental characterization of NBTI so that one can generate parameters for reliability models for sub-0.13 μm technologies that can subsequently be used for statistical VLSI design. Among various experimental techniques used to characterize the parameter shifts, the researchers found an on-the-fly method to provide consistent parameters for NBTI time exponents as well as an absolute level of degradation.
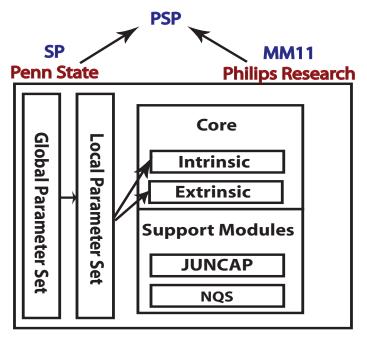
Compact Modeling

Figure 14. Illustration of the SRC-sponsored new "Industry Standard" PSP public domain compact model developed by Penn State and Philips Electronics

A major milestone in 2005 in the compact modeling program was the merger of two new compact models, based on Surface Potential (SP), to form a powerful new compact model for circuit simulators, referred to as PSP. As illustrated in Figure 14, this new model is the combination of the SRC-

sponsored SP model developed by the Gildenb-lat group at Pennsylvania State University (Penn State) and the surface potential model developed by Philips Electronics, MM11. Being completely avail-able in the public domain, this model was recently selected as the new "Industry Standard" MOSFET compact model by the Compact Model Council (CMC) following an exhaustive evaluation of several competing models by several CMC member compa-nies over a period of several months.

Design models for packaging and thermal processes are typically "reduced" or "compact" and need to be fast, adequately accurate, and computationally com-patible with traditional design software. The Joshi group [GIT] has developed and tested a compact model for simulation of interconnect thermal effects that meets all of these requirements. The excellent agreement in numerical values, and the significant reduction in run-time needed with the compact models relative to full thermal solvers demonstrates the advantages of this approach for design applica-tions.

Robust Design Tools and Methods

Microscopic variations in number and location of dopant atoms in the channel region of devices induce increasing electrical deviations in device characteristics, such as threshold voltage. These atomic-level intrinsic fluctuations cannot be elimi-nated by external control of the manufacturing process and are most pronounced in minimum-ge-ometry transistors.

The design of circuits with high yield that meet per-formance specifications in the face of process vari-ability and increased off-state leakage is becoming increasingly challenging as scaling continues. The Roy group [Purdue University] has also provided several solutions for statistical full-chip leakage analysis and transistor sizing through the use of dual oxide thicknesses. This work can effectively improve design quality and yield.

Noise reduction is increasingly important because switching digital circuits produces current peaks that result in voltage fluctuations on the power supply lines due to the inductive behavior of on-chip and chip-to-package interconnects. A new SRC design technique lowers ground bounce in noise

sensitive circuits by 1) adding an on-chip noise-free ground to divert ground noise from the sensitive nodes and 2) utilizing an on-chip decoupling capaci-tor tuned in resonance with the parasitic inductance of the interconnects to provide an additional low impedance ground path. The methodology, which includes a method for determining optimal place-ment of on-chip decoupling capacitors, has shown a reduction of power-grid noise of at least 200% compared to existing methods of placement [Fried-man, Univ. of Rochester].

At the Univ. of California/San Diego (UCSD), the Kahng group has demonstrated layout design techniques which compensate for lithographic focus variation with small area penalties and gate-length biasing techniques, which significantly reduce leak-age and leakage variability[3].

After analyzing Static Random Access Memory (SRAM) cell failures under intrinsic process varia-tion, such as microscopic uncertainties in location and number of dopants, researchers have proposed new variation-aware cache architectures suitable for high performance applications (Figure 15). The proposed architecture adaptively resizes the cache to avoid faulty cells, thereby improving yield. This scheme is transparent to processor architecture and has negligible energy and area overhead. Experi-mental results on a 32K direct map L1 cache show that the proposed architecture can achieve 93% yield compared to its original 33% [Roy, Purdue University].
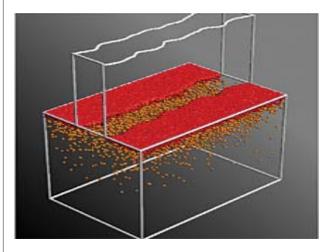

Figure 15. Random doping fluctuations

Much research is aimed at the design of key analog blocks robust to process variation. Analog to Digital Converters (ADCs) play a major role in modern communications circuits. By exploiting protocol redundancy in a calibration algorithm, improvements were seen in the simulated Signal-to-Noise and Distortion Ratio (SNDR) of a 6-bit, 500-MSamples/sec ADC in the receiver of an Ultra WideBand (UWB) system using Orthogonal Frequency Division Multiplexing (OFDM) from 20 dB to 37 dB [Murmann/Wooley, Stanford University].

Mixed-Signal Design

Several SRC researchers have worked to reduce test cost for mixed signal systems. A test methodology has been developed by the Chatterjee group [GIT] for dynamic specification testing of high speed A/D converters on a low cost tester. This alternate test approach avoids the expense of using high-speed Automatic Test Equipment (ATE) by estimating the dynamic specifications of the device on a low cost ATE using an alternate test set-up and mapping functions. Members describe this work as having an impact on addressing the critical challenge of controlling increasing cost for testing analog functions.

Other mixed signal test efforts include development of methods for reducing power/ground noise in high-speed and high-resolution ADC test boards using a novel Electromagnetic Band Gap (EBG) structure. It has been verified with system-level simulations that the suggested EBG structure reduces power/ground noise substantially, resulting in better performance of the ADC [Swaminathan, GIT]. Analog test wrappers for embedded analog cores in mixed-signal SOCs enable analog testing using digital test access mechanisms, thereby reducing the need for expensive mixed-signal testers [Ozev/Chakrabarty, Duke University].

Efficient data conversion is a primary requirement of most modern mixed-signal systems. For example, the Allstot group [Univ. of Washington] designed a 400-MSamples/sec Nyquist rate pipeline analog-to-digital converter implemented in a 90 nm CMOS process, using low-gain operational ampflifiers that are more amenable to the low-voltage environment. Total power is only 139 mW.

A cascade of sigma-delta modulator stages, which employ a feed-forward architecture to reduce the signal ranges required for integrator inputs and outputs, has been used to implement a broadband, high-resolution, oversampling CMOS analog-to-digital converter operating with low-supply voltages. A low-voltage (1.2), low-power sigma-delta modulator integrated in a 0.25 μm CMOS technology achieves a dynamic range of 96 dB for a 1.25-MHz signal bandwidth at a sampling rate of 40 MSamples/sec. The analog power dissipation is 44 mW [Wooley, Stanford University].

Research is under way to study optimized memory architectures for speech recognition that supports an efficient, parallel hardware-based search of the large, layered Hidden Markov Models (HMMs) that are widely used (Figure 16). Two datapath architectures for a hardware-based speech recognition system have been introduced, which use precise memory organization, pipelining, and parallelism to reduce memory accesses and increase performance [Rutenbar, Carnegie Mellon University][1].
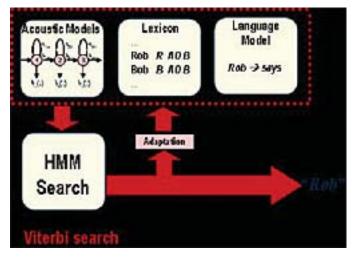

Figure 16. Architecture for hardware speech recognition system

Verification

It is estimated that up to 50% of the total design effort is directed to verification. SRC supported research in formal methods, simulation, and hybrid solutions aims to aid in the behavioral, logic, and physical verification of increasingly complex circuits and systems, including integrated system-on-a-chip, mixed-signal designs, and hardware/software systems. SRC members are seeking to advance verification technology as applied to systems com-

prised of both software and hardware in which the hardware itself is increasingly diverse, composed of multiple independently-developed cores, digital and analog components, processors, memories, a variety of interconnect approaches, system-on-a-chip, and system-in-package.

SRC work in verification expanded into semi-formal verification and coverage analysis and also continued its focus on making theoretically complete but practically intractable methods usable by SRC members. The "gold standard" verification packages are maintained at the Univ. of Colorado so that techniques are kept current with cutting-edge technology, providing a valuable benefit to members. This year these techniques have been expanded to include improved counter-example generation, helping to isolate and correct discovered errors; more effective termination criteria for bounded model checking; and increased efficiency in performance [Somenzi, Univ. of Colorado].

Researchers continue to explore runtime validation techniques for multithreaded processors. They propose a detailed timing simulation of a representative architecture, augmented with run-time validation support. They show in the fault free case that the performance slowdown is only 3% on average. There is little additional performance penalty when the faults are infrequent, which should be the normal case. When the fault rate is 1 per 1,000 cycles, the overall slowdown is 4.13%. As the fault rate drops to 1 per 1 million cycles, the performance is almost equivalent to the fault-free case [Malik, Princeton University][3].

Work in automatic verification of sequential equivalence between two Register Transfer Level (RTL) designs to overcome the state explosion problem faced by reachability-based sequential equivalence verifiers assumes that the two designs are related by certain structural and functional optimizations. In particular, when one design is obtained from another through retiming optimization, the problem is reduced to a structural comparison between the two designs. The process is efficient and scales to very large designs (it was implemented at an industrial site and tested on several large designs.) [Sakallah, Univ. of Michigan][3].

Researchers at the Univ. of California/Santa Barbara (UCSB) have demonstrated experimental techniques that are more efficient than current state-of-the-art combined decision procedures and Boolean SATisfi-

ability problems (SAT) solvers on data-path dominated circuits. Their integrated approach based on automated simplification and powerful proof techniques provides a practical system-level formal equivalence verification checker [Cheng, UCSB].

System Test

Test, as a consideration throughout the design process, is now seen as critical to the three key goals of successful product release: 1) reduced time to volume production; 2) working high-quality reliable parts; and 3) on-target cost. Only by involving test planning and test development in all phases of design and manufacturing start-up can a design be successful. Factors contributing to the added complexity (and increased importance) of test include shortening time-to-market requirements, Moore's Law effects of higher densities and more complex devices, higher frequencies and clock rates, phase correction alter mask layout, and system-on-chip design with components from multiple sources. SRC test efforts span digital, analog, RF, and mixed signal technologies.

Efficient and cost effective test is key to reducing both the one-time test pattern generation cost and the re-curring test application cost. Yield loss minimization is the goal of the Reddy group [Univ. of Iowa] on new methods to model metal line opens and bridges in VLSI designs using multiple line stuck-at faults. These techniques reduce test cost by avoiding overtesting and compressing test data for Deep SubMicron (DSM) designs.

Work on multiple-defect test sets is filling the gap between the simplicity of the stuck-at fault models and the thoroughness of targeting complex defect types. By generating several tests for the same stuck-at fault, the chances of activating a complex defect involving the targeted line increases. Considering the state of the signal lines in close physical proximity to the targeted stuck-at fault helps determine whether a test is new. A test generation algorithm that uses this metric to establish many unique neighborhood states will detect more defects and lead to fewer defective shipped products than current techniques and is benefiting SRC members [Blanton, Carnegie Mellon University].

Power Management

As indicated earlier, power consumption and associated thermal management requirements are

increasingly important concerns. There is substantial leverage to be gained in power management via design methodology. Researchers at UCB have tested the mixed-signal baseband chip for wireless sensor networks. Measurement results show that the overall circuits draw about $200\mu A$ of current from the 1.0 V supply. By externally setting lower bias currents, the baseband is still able to synchronize with a power consumption as low as 120 μW [Sangiovanni-Vincentelli, UCB][3].

Work in a design methodology for synchronization in wireless communication has yielded significant improvements in both energy consumption and convergence time of 4-10x in representative problems of carrier frequency recovery and timing recovery respectively. This synchronization system for a wireless sensor network consumes less than $300\mu W$ (including the ADC). This is so low that further reduction would have very little system impact [Irwin, Penn State][3].

A novel transistor level leakage optimization approach achieves leakage power reductions of 23% (average) and 43% (maximum) without any delay increase and with negligible impact on the active power [Najm, Univ. of Toronto]. Other work yields result from the practical implementation of a power optimization paradigm for sequential components, reducing both dynamic and leakage power consumption on a significant number of industrial test cases [Macii, Politecnico di Torino].

Even when inactive, SRAMs can consume a large percentage of power; and since they are also highly susceptible to process variations, work on reducing SRAM power must also comprehend system robustness. The Roy group [Purdue University] has shown that it is possible to combine device, circuit, and architecture level techniques to offer 64% total leakage reduction and 7.3% improvement in bit line delay without impacting the cell stability compared to previous state-of-the-art, low-leakage cache SRAM techniques.

Design Productivity

Incremental improvements in design productivity are no longer sufficient to keep pace with the increasing complexity, both of designs and the factors with which designs must contend – variability and other manufacturing-related factors, power, aggressive cycle times demanded by customers, and aggressive

time-to-market requirements. Increased productivity must come from orders of magnitude improvements in speed and ease of use of tools, especially in moving design to a higher level. System-level design, with the challenges of accurate estimation and the ability to "see" down to the circuit level and below, is key to productivity improvement, but it has also been difficult to achieve.

Phase-Locked Loops (PLLs) and Voltage-Controlled Oscillators (VCOs) are critical units in a variety of mixed-signal and digital systems, ranging from communications and wireless applications to disk drives and microprocessors, and are sensitive mixed-signal components whose imperfections have a disproportionately large impact on overall system performance. With device sizes shrinking, second-order effects increasing in importance, and undesired coupling becoming increasingly significant, it is essential during design to verify these blocks with high accuracy. Related work has resulted in macromodel generation algorithms for oscillators and PLLs, multi-time simulation algorithms, and a system-level methodology that shows superior accuracy and 2 to 3 orders of magnitude speedup over SPICE (Figure 17) [Roychowdhury, Univ. of Minnesota].
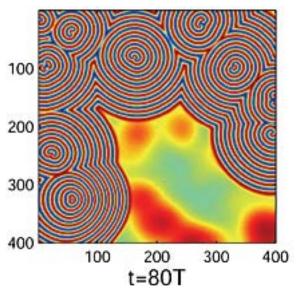

Figure 17. 1000x simulation speedup for 160,000 coupled Brusselator oscillators

With clocking becoming increasingly challenging as we continue with scaling, a new clock network synthesis technology is being developed for high chip complexity in hierarchical/SoC designs. Experimental results on benchmark circuits show that an

approxmate 50% clock net wirelength reduction can be obtained through a simple, yet effective, method using intentional skew routing and clock buffer blockage avoidance [Hu, Texas A&M University].

As technology scales to 0.13 micron and below, designs are requiring buffers to be inserted on interconnects of even moderate length for both critical paths and fixing electrical violations. Consequently, buffer insertion is needed on tens of thousands of nets during physical synthesis optimization. Approximation techniques, also developed by Hu's group, have been shown to provide solutions to repeater insertion up to 25 times faster than existing techniques with less than 3% delay penalty. This is important as interconnect delay becomes the dominant part of the overall delay [Hu, Texas A&M University].

New tools for power and reliability estimation at the system level and a multi-processor SoC simulation environment in an industry standard language, System C, to support architecture definition and enable system optimization have been developed. These tools include cycle accurate power models and combined memory/interconnect optimizations and will be most useful in exploring different configurations in future multi-processor systems [Irwin, Penn State].

Higher-level design is critical to continuing to improve designer productivity. A flow to synthesize concurrent communicating systems while optimizing inter-process communication is being developed. With this flow, it is easy to incorporate IP blocks and develop communication latency constraints through querying simulation traces (limiting manual interaction to avoid human errors). This work further bridges the gap between behavioral level synthesis and system level design [Sangiovanni-Vincentelli, UCB][3].
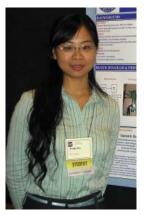
Nearly 1,000 students participated in SRC-funded research in 2005; over 500 participated in MARCO/FCRP-funded research. Of SRC students graduating in 2005, 66% went to work for SRC member organizations or are undergraduate or master's students continuing to advanced degrees, further strengthening the links within the SRC community. For MARCO students graduating in 2005, 60% went to work in sponsoring organizations or are continuing to an advanced degree. Other 2005 accomplishments included:

- Five new Core Fellowships and four new Company-Named Fellowships were awarded through the Graduate Fellowship Program to bring the number of Fellows to 38 at the beginning of the 2005 fall term. Eleven SRC Fellows graduated in 2005.
- Seven new Company-Named Master's Scholarships were awarded, for a total of 19 at the beginning of the 2005 fall term. Six Master's Scholars graduated in 2005.
- 158 SRC students presented their research at TECHCON 2005 in Portland, OR (see TECHCON 2005, p. 25.)
- Student Relations published 674 individual resumes on the SRC web site, and another 308 on the MARCO web site.
- The annual Student Programs Brochure was published to provide student information for members and prospective Fellows and Scholars. A copy may be obtained by contacting SRC Student Relations at the SRC corporate address.
- The fifth Simon Karecki Award was made from the Simon Karecki Fellowship Fund to Subramanian Tamilmani, Univ. of Arizona. This award recognizes outstanding student performance through the SRC/NSF Center for Environmentally Benign Semiconductor Manufacturing, centered at the Univ. of Arizona.
- MARCO/FCRP student/industry networking events were held in conjunction with annual research reviews for the FENA, C2S2, MSD, IFC, and GSRC Focus Centers.
- TechConnects for SRC students were held at the Univ. of California/Irvine, Stanford University, and North Carolina State University.
- Phase 1 of the SRC/SIA SoC Design Challenge culminated at TECHCON 2005 in the presentation of awards for first, second and third place to research teams from the Univ. of Virginia,

Harvard University, and Michigan State University, respectively. These teams and teams from the Univ. of Tennessee and Tufts University will participate in Phase 2 through 2006.
- A Student Handbook was published on the SRC and MARCO web sites to help students better understand how to interact with SRC and MARCO and to take advantage of opportunities available through SRC and MARCO.

The team from the Univ. of Virginia took first place in Phase 1 of the SRC/SIA SoC Design Challenge. Team member Wenqian Wu is shown with the team's poster at TECHCON 2005 in Portland, Oregon

SRC Education Alliance

The SRC Education Alliance (SRCEA), a wholly-owned subsidary of the SRC, is a non-profit private foundation under IRC sections 501(c)3 and 509(a). The Undergraduate Research Assistants Program (URA) is managed through the SRCEA with funding from the Department of Defense and MARCO. The URA Program targets academically qualified students early in their undergraduate careers and seeks to build their enthusiasm for disciplines of interest to the semiconductor industry.

Thirty-four students at 11 universities participated in the URA program in 2005. Eight students completed the program of whom five continued to graduate school and two joined sponsoring organizations. Twenty-one students are currently in the program. A highlight of the program was the presentation of posters by three of the students at TECHCON 2005.

Anne Friedman (front), URA student at Penn State, puts up her poster at TECHCON 2005 with help from SRC Fellow, Lisa Edge, also from Penn State

SRC students vied for Best in Session Awards as they presented 158 papers in 20 sessions at TECHCON 2005 in Portland, Oregon. The SRC's seventh technical conference was held at the Portland Marriott Downtown on October 24 – 26, 2005, and provided a forum for reviewing a major portion of the SRC research portfolio and networking among industry, faculty, and students in TechFair and CareerConnections.

Dr. John Warlaumont (l), Director of IBM"s Semiconductor Technology Lab and SRC Board Chair, presented the Best in Session Awards at TECHCON 2005

Three invited sessions added value for 442 attendees. Nine students from the Focus Center Research Program presented their research, as did winners of Phase 1 of the SRC/SIA SoC Design Challenge. A highlight of the Conference was an invited session on Biologically Inspired Silicon.

A highlight of TECHCON 2005 was a special session on Biologically Inspired Silicon. Speakers included (l-r) John Granacki and Theodore Burger of Southern Cal, Ralph Cavin (SRC), Richard Granger of UC Irvine, and Dan Hammerstrom of Portland State (session chair)

Invited speakers from the industry included Novellus CEO and Chairman Richard Hill who delivered the keynote address. Dr. Bernard Meyerson addressed the Graduate Fellows and Master's Scholars

at the Graduate Fellowship Program Annual Conference Banquet. Luncheon speakers included AMD's Chuck Moore and Intel's Robert Chau. SRC student alumnus Dr. Ward Engbrecht spoke at the Awards Luncheon.

TECHCON 2005 also provided a forum for recognizing excellence within the SRC community. TAB Chair, Inventor Recognition, and Mahboob Kahn Outstanding Mentor awards were presented at the conference banquet. The 2005 Technical Excellence Award was presented to Professor Kaushik Roy and several of his students from Purdue University. The 2005 Aristotle Award was presented to Professor David Allstot, Univ. of Washington, and the first Faculty Leadership Award was presented to Professor Toh-Ming Lu, Rensselaer Polytechnic Institute.

The SRC Booth was a busy place at TECHCON, especially when students were loading their presentations with the help of SRC staff on Sunday evening

IBM/SRC Fellow Oluwafemi Ogunsola, GA Tech, discusses his research with Harold Hosack, SRC Director for Interconnect and Packaging Sciences

Professor David Allstot (center), winner of the 2005 Aristotle Award, with current student and SRC Fellow Charles Peach (left), and former student and current SRC funded investigator Terri Fiez

Aristotle Award

The 2005 Aristotle Award was presented to Professor David Allstot, of the Univ. of Washington, at TECHCON 2005. The Aristotle Award recognizes SRC-supported faculty whose deep commitment to the educational experience of SRC students has had a profound and continuing impact for SRC members over a long period of time. The award acknowledges outstanding teaching in its broadest sense, emphasizing student advising and teaching during the research project.

Mahboob Khan Award

The Mahboob Khan Outstanding Mentor Award, named in memory of a long-time SRC Industrial Liaison program advocate from Advanced Micro Devices, is presented each year to those individuals who have made significant contributions in their roles as Industrial Liaisons. Recipients represent "ideal mentors" whose commitment more than enhances the SRC research program.

The 2005 award recipients were:

Ching Tsun Chou of Intel was nominated by SRC researcher, Ganesh Gopalakrishnan of the Univ. of Utah, for his special ability to lead and mentor student researchers. According to Dr. Gopalakrishnan, "Ching Tsun's attention to detail, turnaround time for responses, and brilliance of insights offered, are of the highest quality. His style of offering these insights is also least disruptive in the sense it is offered as if we thought of it, or helped think about it, when in reality the idea might have been nearly 100 percent Ching Tsun's own."

Keith Green of Texas Instruments was nominated by Professor Juin J. Liou of the University of Central Florida for his work with a task titled, "Isolated Top and Bottom Gate Junction Field-Effect Transistor Model for Computer-Aided Circuit Design." This task deals with modeling of the four-terminal junction-field transistor (JFET). During his weekly teleconference with students at Central Florida, Keith tirelessly provided guidance, directions, and experimental data. During the summers of 2004 and 2005, Keith arranged for student internships at Texas Instruments.

Susheel Jadhav of Intel was nominated by Professor Indranath Dutt of the Naval Postgraduate School (NPS) for his long and active collaboration with the Miniaturized Impression Creep Test for BGA and FC Solder Joints task. Susheel has been part of the research team since the task began in 2002. During that time he has made quarterly visits to NPS, usually spending one full day in the lab with student researchers, Robert Marks and Deng Pen, during each visit. Mr. Jadhav hosted an internship for Dr. Marks at Intel's Chandler facility, enabling him to conduct experimental work related to the SRC supported research task. Because of his sustained involvement, tests developed at NPS are being transferred for industry use.

Mike Lamson of Texas Instruments has worked with the packaging research program at the Univ. of Arizona since the late 1980's. He has encouraged a generation of students to pursue advanced degrees. According to Professor John Prince, he has "provided significant guidance to carrying out research into modeling and simulation of interconnect performance." According to nominator Allen Bowling of Texas Instruments, Mike has "actively provided test structures to make the results most useful to TI and industry."

Phil Nigh of IBM was nominated by Professor Shawn Blanton of Carnegie Mellon University for his long term relationship with SRC's research community. Dr. Nigh has conducted "regular teleconference meetings (at least twice a month and sometimes even once a week) to discuss the plans and progress made towards "executing" the project on real-life chips. He has connected several SRC research task participants with test and design data so they can execute their current methodologies on chips currently in production. Dr. Hank Walker of Texas A & M describes Phil as "everything we want a

good mentor to be - enthusiatic, patient, encouraging, teaching, and learning."

Adam Pawloski of AMD worked with Dr. Grant Willson and his large group of students at the Univ. of Texas at Austin. As an alumni of SRC's Graduate Fellowship Program, Dr. Pawloski is a role model as he develops relationships with current SRC students. Nominator Grant Willson notes that "his input on the design of the experiments has been invaluable not only to the research, but also to the growth of the students involved in the project." Dr. Pawloski has been especially proactive in introducing students to the work environment at AMD, enabling many to experience and be exposed to state-of-the-art tools and industry practices.

Koneru Ramakrishna of Freescale has a long history of working with the university community. Currently, he is working with Professors William King and Yogendra Joshi at Georgia Tech on their task titled, "Electron Transport Size Effect and Joule Heating in Nanoscale Metallic Interconnects Embedded in Novel Low-k Dielectric Materials." He established a particularly close relationship with SRC supported student, Siva Gurrum. According to nominator, William King, "Mr. Gurrum received specific guidance on the direction of his research and general guidance on the career choices he has been making."

Technical Excellence Award

The SRC Technical Excellence Award is given annually to researchers who, over a period of years, have demonstrated creative, consistent contributions to the field of semiconductor research; who are ground-breakers and leaders in their fields; and who are regarded as model collaborators with their colleagues in the SRC member community. The award is shared by researchers who have made key contributions to technology that significantly enhance the productivity of the semiconductor industry.

The 2005 Technical Excellence Award was presented by SRC Board of Directors Chairman, John Warlaumont at the TECHCON 2005 Awards Banquet.

This year SRC selected Professor Kaushik Roy of Purdue University and his team of 11 student researchers. They were chosen for their investigations in the various aspects of device/circuit and architecture design for ultra low power digital sub-threshold operations. Over the past 10 years, Dr. Roy's leadership has resulted in many Best Paper Awards and numerous publications by him and his student researchers.

SRC Faculty Leadership Award

At its June 2005 meeting, the SRC Board of Directors created a new award, the SRC Faculty Leadership Award, to recognize leadership exhibited in management of a large, dispersed, SRC-sponsored research program requiring collaboration among multiple universities and faculty from multiple disciplines.

The first SRC Faculty Leadership Award was presented at the TECHCON 2005 banquet to Dr. Toh-Ming Lu, Professor of Physics at Rensselaer Polytechnic Institute. He was chosen to receive the initial award for his work as the Director of the Center for Advanced Interconnect Science and Technology (CAIST). The center began in 1996 under Dr. Lu's leadership and grew to include 15 universities and 50 task leaders. The center seeks to evaluate the new and innovative strategies that are critically required not only to push to the limits of Si scaling, but also to address many technology bottlenecks for future heterogeneous Si systems which will continue Moore's Law beyond scaling limits.

Intellectual Property (IP) assets emerging from SRC sponsored university research programs are provided by SRC to its members to protect and enhance the value of SRC membership. IP assets serve to support SRC's mission and charter to transfer and commercialize the results of SRC sponsored research programs by SRC member companies. SRC's significant portfolio of intellectual assets minimizes the risk of infringement and encumbrances as research results are utilized by industry. Accordingly, SRC member companies are given the freedom to practice, use, and commercialize the results of research programs funded through SRC sponsorship. IP assets are integrated with the SRC research catalog and complement the value chain as an important benefit of SRC membership.
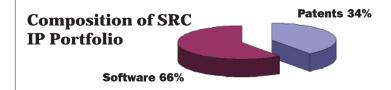
In return for sponsorship, SRC receives non-exclusive, worldwide, royalty free licenses to IP from university research programs funded by SRC. These IP rights are transferred contractually as applicable to SRC member companies. Rights in patents, copyrights, software, databases, and other IP, such as mask registrations, are obtained as required to allow SRC members to practice and use the results of SRC-sponsored research. As an additional service to members, access to background intellectual property licenses necessary to practice SRC research results may be investigated, whether the background IP is from an industry or academic source. While SRC IP exists primarily for defensive purposes, SRC enforces its IP rights as necessary to provide a level playing field for members by ensuring that those who utilize SRC sponsored technologies do so only within the scope of a valid license. SRC also seeks to ensure that members receive and benefit from all IP rights resulting from SRC research to which they are entitled.

SRC continually investigates ways in which IP assets can provide new and additional sources of value to the SRC member community. In an effort to build a themed IP portfolio, SRC recently pioneered an innovative joint licensing and commercialization partnership focused on oselected inventions in specific technology areas. The Exclusive Licensing Model has received strong support from several universities and member companies. This new program significantly benefits SRC members by increasing their potential competitive advantages while also providing for a possible new source of royalties. Under this new licensing model, select SRC and university intellectual property rights are combined and licensed to SRC. The formerly separate IP rights have greater value once combined in an escrow managed by SRC. As a result, enhanced commercialization prospects and greater licensing value can be provided as compared with the traditional SRC-university licensing model. The university, SRC, and SRC member companies agree on terms to sub-license one or more companies able to commercialize the invention and share the royalties collected. SRC, SRC member companies, and several universities have been working together to implement this new experimental licensing model. In 2005, a first agreement was executed with Duke University seeking to develop an SRAM technology based IP themed portfolio.

During 2005, 14 SRC-sponsored U.S. and foreign patents were issued. This brings the total portfolio of SRC issued patents to 247. SRC's significant patent portfolio supports both U.S. and international member company operations in numerous countries around the world. SRC's web site permits members to submit real-time queries into SRC's IP database to obtain status on pending and issued patents as well as information on SRC sponsored software.

The SRC IP portfolio also provides over 491 software programs, software models, and technical databases to member companies. Software and database licenses from SRC-sponsored research programs represent a growing and complementary part of the SRC IP portfolio. Members are directed to the online software directory at URL http://www.src.org for further details. SRC members receive non-exclusive, worldwide, royalty-free intellectual property licenses for applicable software programs and technical databases.

Composition of SRC IP Portfolio

Patents 34%

Software 66%

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Supermolecular Structures and Devices Made from Same	Daniel Herr Victor Zhirnov	14-Oct-03 24-May-05	6897470	SRC North Carolina State University
Patterning Methods and Systems Using Reflected Interference Patterns	Daniel Herr David Joy	9-Mar-04 22-Nov-05	6967067	Univ. of Tennessee at Knoxville
Electrical Device Including Dielectric Layer Formed By Direct Patterning Process	Daniel Herr Karen Gleason Chris Ober	23-Oct-02 20-Sep-05	6946736	SRC MIT Cornell University
Buried Solder Bumps for AC-Coupled Microelectronic Interconnects	Paul Franzon Stephen Mick John Wilson	7-Oct-04 9-Aug-05	6927490	North Carolina State University
Optoelectronic Devices Having Arrays of Quantum Dot Compound Semiconductors Superlattices Therein	Salah Bedair Veena Misra Mehmet Ozturk Zhibo Zhang	20-Jan-04 5-Jul-05	6914256	North Carolina State University
Increase of Integrated Antenna Gain by Inserting a Low Loss, High Thermal Conductivity Dielectric Layer Between Chip and Heat Sink	Xiaoling Guo Ran Li Kenneth O	10-Jun-03 11-Jan-05	6842144	University of Florida
A Stabilization Technique for Phase-Locked Frequency Synthesizers	Tai-Cheng Lee Behzad Razavi	29-Jan-03 8-Mar-05	6864753	University of California at Los Angeles
High/Low Work Function Metal Alloys for Integrated Circuit Electrodes and Methods of Fabricating Same	Shinnam Hong Veena Misra Huicai Zhong	22-Feb-02 29-Mar-05	6873020	North Carolina State University
Inductively Coupled Electrical Connectors (As Amended)	Paul Franzon Stephen Mick John Wilson	28-Nov-01 26-Apr-05	6885090	North Carolina State University
Charge-Based Frequency Measurement BIST for PLL	Seongwon Kim Mani Soma	23-Sep-99 26-Apr-05	6885700	University of Washington
Multiple Copper Vias for Integrated Circuit Metallization and Methods of Fabricating Same	Paul Ho Ki-Don Lee Hideki Matsuhashi Ennis Ogawa	15-Oct-02 19-Jul-05	6919639	University of Texas at Austin

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Multiple-Thickness Gate Oxide Formed by Oxygen Implantation	Chenming Hu Tsu-Jae King	5-Sep-01 15-Feb-05	6855994	University of California at Berkeley
Methods for Removing Contaminants on a Substrate	M. Quevedo-Lopez Robert Wallace	21-Nov-02 23-Aug-05	6933235	University of North Texas

Foreign Patent

Title	Inventor(s)	Filing Date Issue Date	U.S. Patent Number	University
Supermolecular Structures and Devices Made from Same	Daniel Herr Victor Zhirnov	23-Feb-01 1-Apr-05	1230406 Taiwan	SRC North Carolina State University

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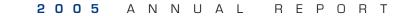
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Financial report available on request.

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