1985 Annual Report

COOPERATIVE RESEARCH

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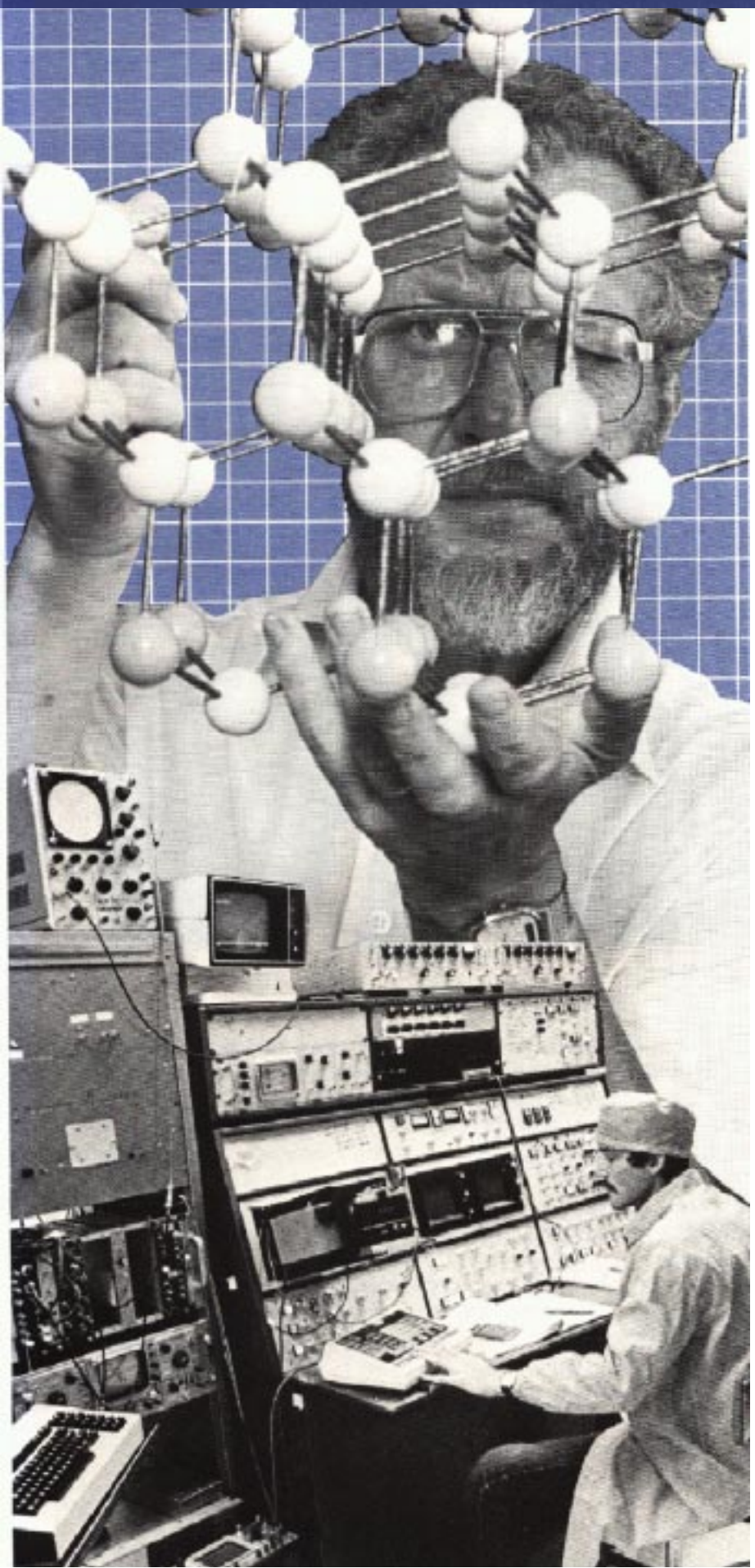
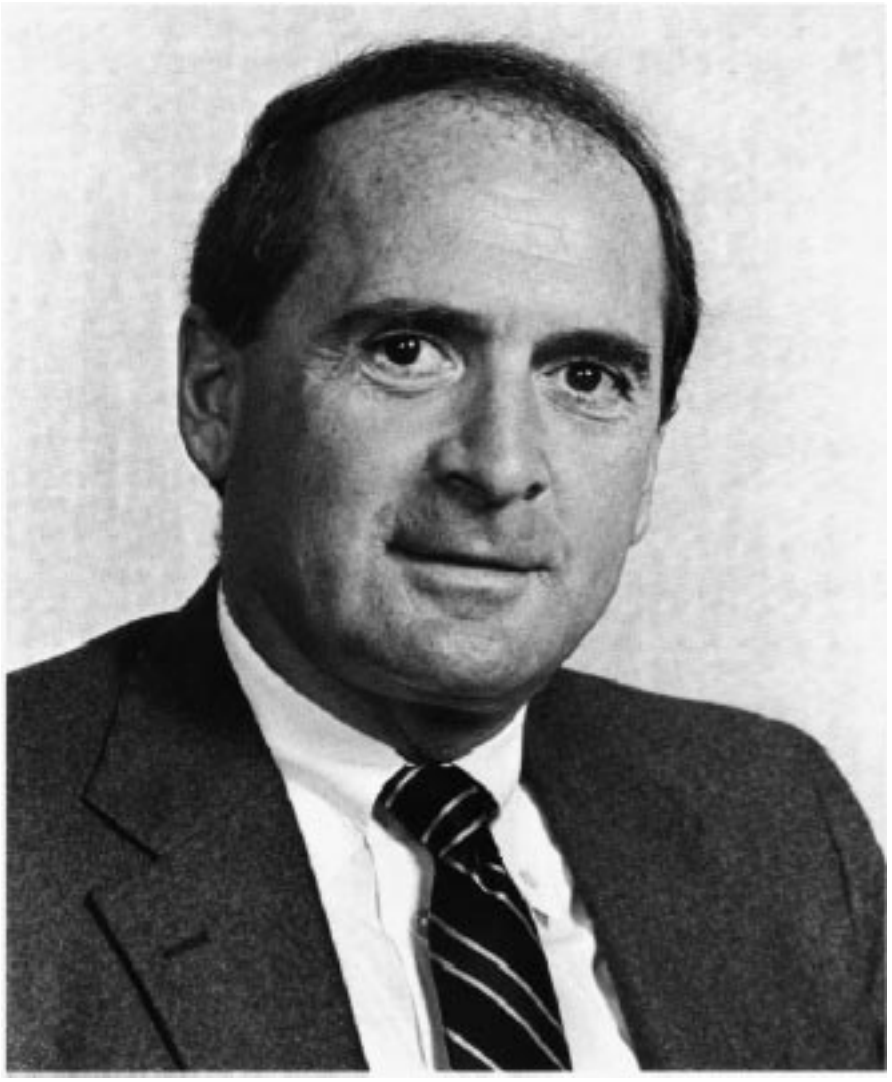
1985 Annual Report



Semiconductor Research Corporation

The Semiconductor Research Corporation (SRC) is a cooperative, formed in 1982 by U.S. companies, that addresses generic research and educational needs (primarily through a university-based, contract research program) related to the design, development, and production of integrated circuits in order to enhance the competitiveness of its members.

Message from the Chairman of the Board and President



George M. Scalise

This third annual report describes a vibrant and productive cooperative research program. In this introductory letter, the most salient aspects of the SRC, present, past, and future, are described from our perspective.

In the last three years, much has been accomplished by the SRC. The research agendas of universities are very much different from what they would otherwise be, internal activities of some member companies have been markedly affected by participation in the SRC, a significant number of students who have participated in our university research are now working in the industry, and barriers to cooperation have been reduced. Useful research products are appearing regularly. On its present course, the research program will result in a rapid increase of such impacts. We should take collective pride in what has been accomplished. The SRC is making a big difference.

In 1985, the semiconductor industry experienced the most severe reduction in sales in its history. That the SRC survived without major impact on its research or membership attests to the

Larry W. Sumney

positive image it has established among its members and their strong commitment. In fact, the year was a good one for the SRC. Dr. Howard Phillips joined the staff to solidify the complement of experienced program directors that effectively manage the research program. Equally important has been the addition of two industrial residents to the staff, Dr. Shakir Abbas from IBM and Phil Lutz from General Motors. Manufacturing science research has become a focal area for program growth. The planned expansion of the packaging research program was on schedule. Design software is advancing rapidly. The quarter-micron technology thrust took a major step forward with a benchmark research conference. Management of the program matured with the development of technology roadmaps that lead to the achievement of the research goals. Our confidence in cooperative research was confirmed by a recent comparative evaluation which concluded that quality is an inherent attribute of the SRC research program because of the selection, management, and review procedures that are applied.

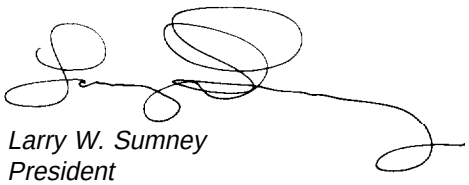
Most importantly, the output of the research is reaching the level expected by its originators.

The SRC is not, in its present form, a complete response to the long-range problems of the U.S. semiconductor industry. It was not planned to be. However, it does demonstrate that cooperation works. The SRC exhibits all of the attributes of a successful cooperative venture.

It is now proper to ask what can be done to extend the success story of the SRC to obtain a greater impact on the competitiveness of the U.S. semiconductor industry. This is addressed in the recently adopted SRC Long Range Plan. Already, the SRC is extending its activities beyond technology into education and into activities that address manufacturing equipment issues. We see the future as one in which the SRC reaches into new areas to help the industry identify and address common needs at all levels.

In our perspective, the SRC is more than a small core staff; it is an amalgamation of the interests and efforts of many people and organizations. Well over 1000 people and over 100 organizations are involved. Our confidence in the ability of the SRC to materially contribute to preservation of U.S. leadership in microelectronics is unshakable. We are proud to be working with you.

George M. Scalise
Chairman, Board of Directors



Larry W. Sumney
President

Précis

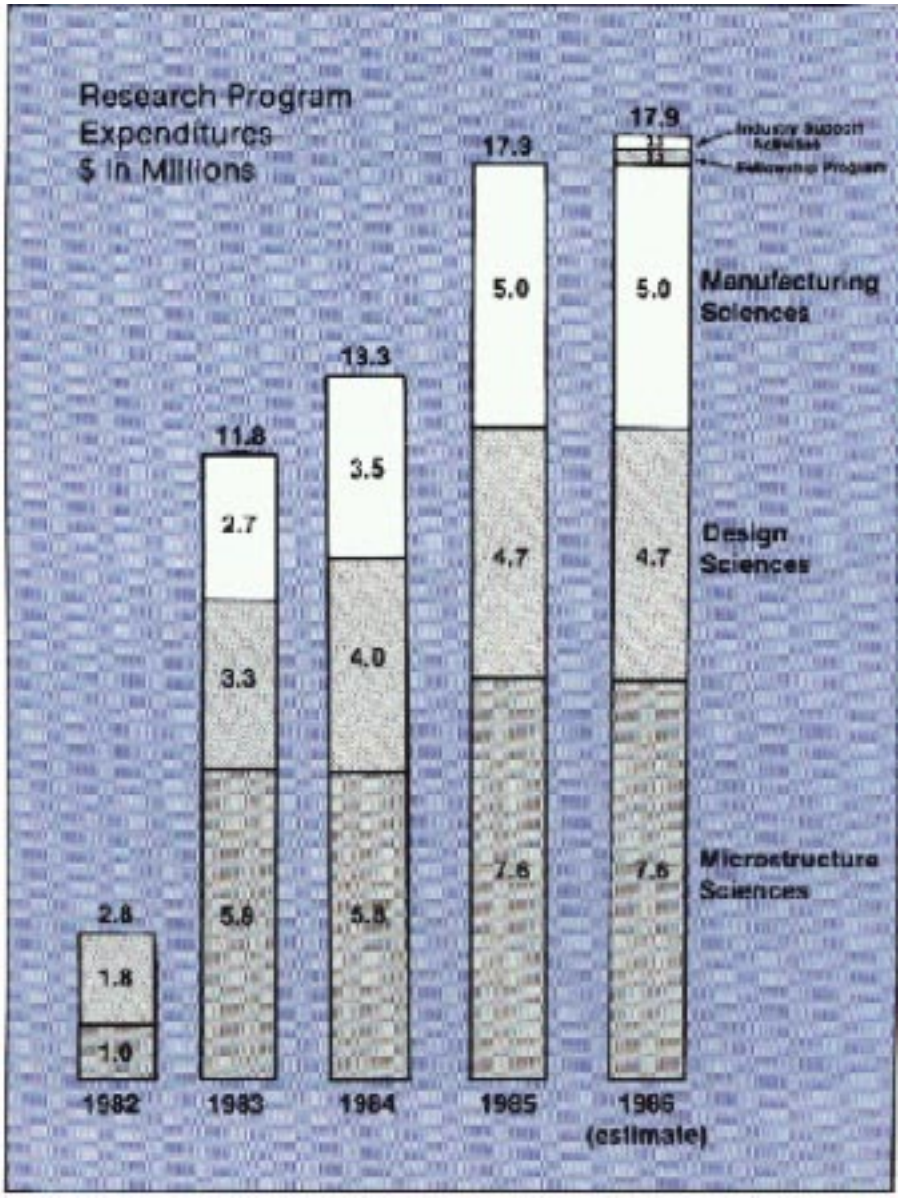
The Semiconductor Research Corporation was established in response to a realization by U.S. companies with interests in integrated circuits that it was becoming necessary to cooperate in order to maintain the vitality and competitiveness of the U.S. semiconductor industry. Cooperation implies, by its nature, more effective ranking of priorities in the activities covered, increased efficiency in their performance, and increased competition in those areas that remain proprietary. The first area chosen for cooperation is support of university research and graduate student training. In response, the initial SRC mission has been to plan and implement a research program, principally at universities, using funding provided by the member companies. Coordination and prioritization is achieved with the help of a Technical Advisory Board, and the research is accomplished through actively monitored contracts with emphasis on rapid transfer of the results to the industry, The educational objective is met through the involvement of graduate students in the research.

The research program of the SRC is directed toward making the U.S. semiconductor industry more competitive in the world marketplace by:

** Creating and maintaining a generic research base in integrated circuit technologies in the U.S. university community,,*

** Insuring a continuing supply of highly qualified students (and the faculty required to educate them) to support the growth and continuing innovation of the industry;*

** Broadening the U.S. university base of microelectronic research and education through establishment of centers of excellence, seeding of new efforts, and development of new curricula.*



Based on the needs of the industry, the core research program will be supplemented by other activities that are consistent with the SRC mission and do not detract from the core research, and for which the SRC is the best available mechanism for undertaking the activity.

From its initial eleven founding companies in 1982, the membership expanded to 35 by the end of 1985. This includes a chapter member which is an association of 33 smaller equipment and materials suppliers. The cumulative research commitment exceeds $45 million. The twenty-five person staff of the SRC includes three industrial residents on assignment from member companies. This staff, working closely with the Technical Advisory Board, interfaces with over 40 universities in order to implement and carry out research. This staff also conducts an intensive technology dissemination effort to deliver research output to the technical staffs of members. A computer-based system is used for information dissemination and communications with the SRC constituency, both in industry and the universities.

Industry Environment

The industry environment in which the SRC will be participating over the next decade can be characterized as follows:

Competition

International competition will increase in intensity, particular/y from the Pacific rim nations (Japan, Taiwan, and Korea) and Europe. The USSR and the People's Republic of China are not considered to be significant factors in this period. The U.S. must concede continuing advantages to foreign competitors in the cost of labor, cost of capital, and the quality of labor/ management as manifested by a cultural dedication to quality, loyalty, and output.

U.S. Government Policy

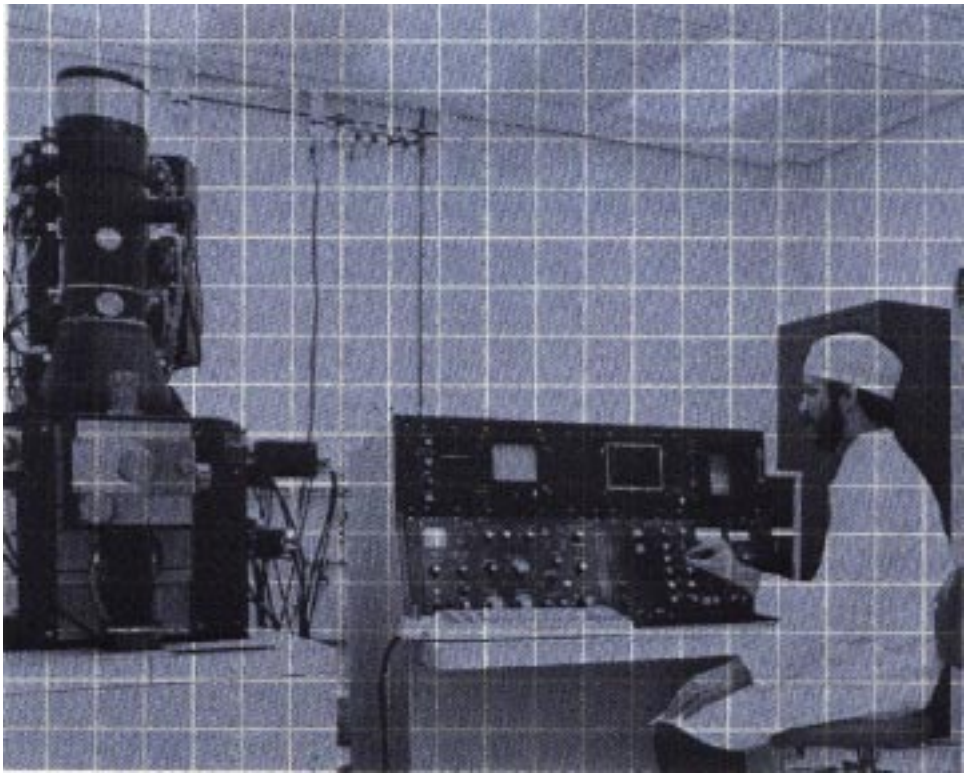
It is unlikely that a comprehensive U.S. industrial policy and/or strategy will be developed in this period. Foreign ownership of U.S. firms or establishment of U.S. operations by foreign companies will continue unabated. Protectionist measures will likely increase as competition intensifies. More attention to environmental controls could increase the cost of manufacture. However, the legal and tax structures will probably continue to be relaxed to permit or encourage more cooperative activities with increased government involvement or support.

Products

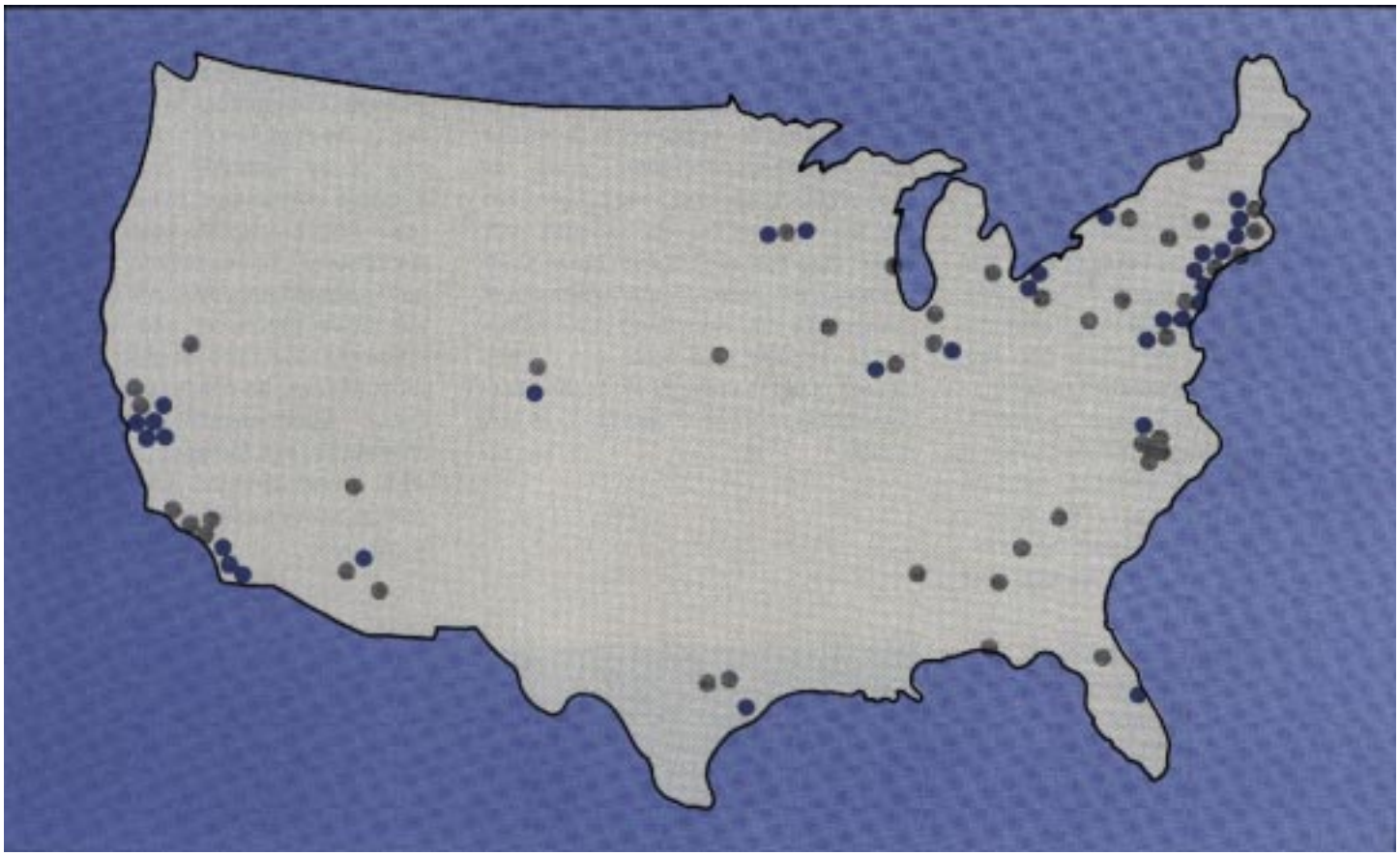
Product complexity and device density will continue to increase. High volume commodity products (memory) will continue to experience pressure from overseas suppliers while increased U.S. attention will be given to application-specific ICs (ASICs) with lower volumes and higher value. This will require significant improvements in design time and more flexible manufacturing facilities and tools. No unpredicted radical change in technology (stochastic shock) is foreseen in this period.

Industry Structure

The IC industry will consolidate to spread R&D and manufacturing costs. Weaker competitors will either drop out, or be acquired by foreign competitors or by vertically integrated U.S. systems companies (who may serve open and/or captive markets). Standardization, particularly of manufacturing equipments and unit processes, will likely increase; and equipment suppliers will tend toward narrower product lines and increasing specialization. Subcontracting of standard operations (e.g., foundries) will increase with proprietariness shifting toward design as opposed to manufacturing know-how.



Participants



Institutions

Arizona, University of
Arizona State University
Auburn University
Brown University
California at Berkeley, University of
California at Los Angeles, University of
California at Santa Barbara, University of
California Institute of Technology
Carnegie-Mellon University
Case Western Reserve University
Clemson University
Colorado State University
Columbia University
Cornell University
Duke University
Florida, University of
Florida State University
Georgia Institute of Technology
Illinois at Urbana/Champaign, University of
Iowa, University of
The Johns Hopkins University
Lehigh University
Massachusetts Institute of Technology
Michigan, University of
Microelectronics Center of North Carolina
Minnesota, University of
Mississippi State University
Nebraska at Lincoln, University of
North Carolina at Chapel Hill, University of
North Carolina State University
Notre Dame, University of
The Pennsylvania State University
Purdue University
Rensselaer Polytechnic Institute
Research Triangle Institute
Rochester, University of
Southern California, University of
Stanford University
Texas at Austin, University of
The Texas A&M University
Vermont, University of
Wisconsin, University of
Yale University

Companies

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Advanced Micro Devices, Incorporated
Burroughs Corporation
Control Data Corporation
Digital Equipment Corporation
E.I. du Pont de Nemours & Company
E-Systems, Incorporated
Eaton Corporation
GCA Corporation
GTE Laboratories, Incorporated
General Electric Company
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Harris Corporation
Hewlett-Packard Company
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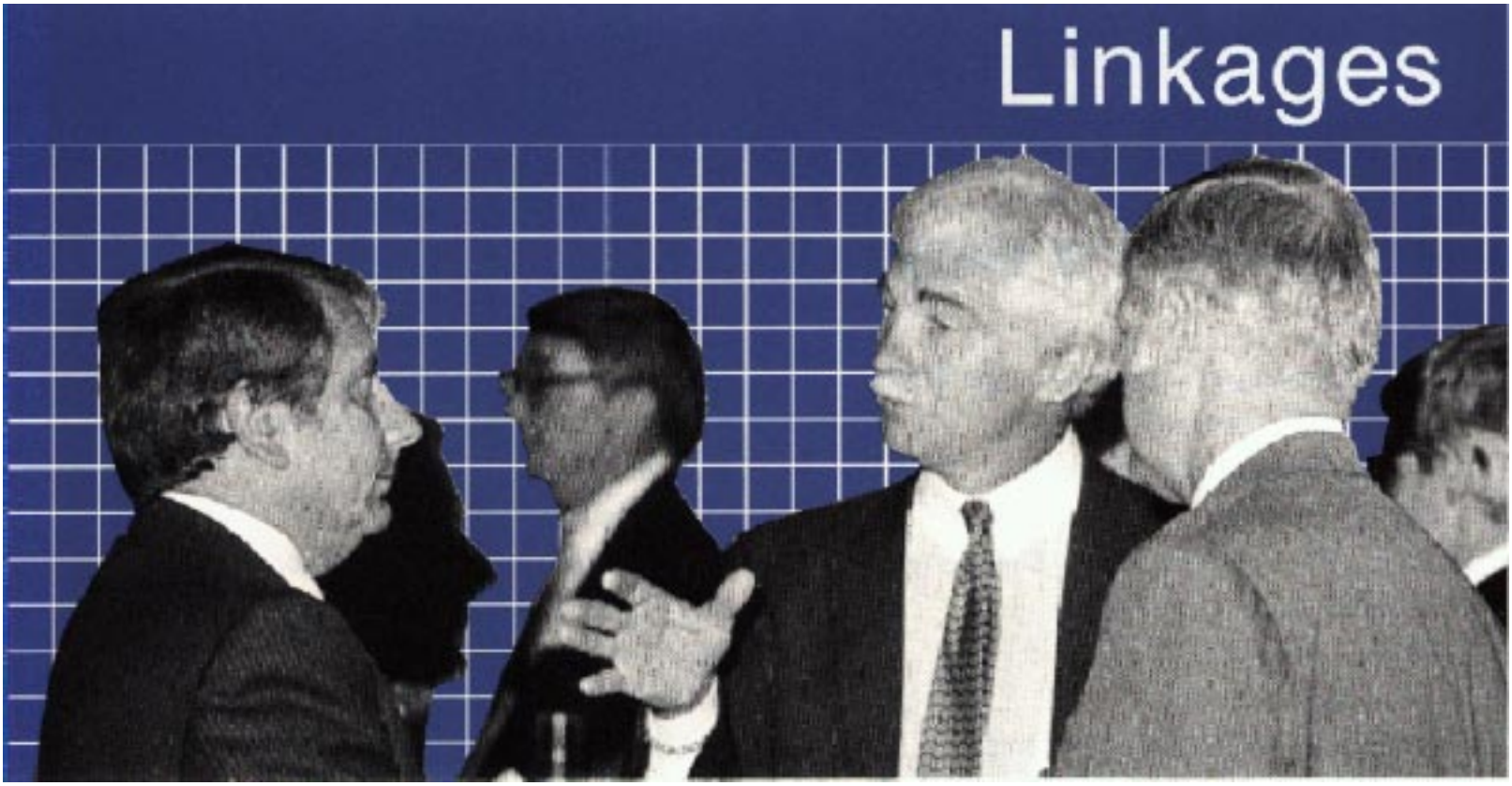
Intel Corporation
Eastman Kodak Company
LSI Logic Corporation
Monolithic Memories, Incorporated
Monsanto Company
Motorola, Incorporated
National Semiconductor Corporation
The Perkin-Elmer Corporation
RCA Corporation
Rockwell International Corporation
*SEMI, Chapter**
Silicon Systems, Incorporated
Sperry Corporation
Texas Instruments Incorporated
Union Carbide Corporation
Varian Associates, Incorporated
Westinghouse Electric Corporation
Xerox Corporation

**The following companies are included in the Semiconductor Equipment and Materials Institute, Inc., Chapter:*

Dynapert/Amedyne
Eagle-Picher Industries, Inc.
E/G Electra-Graph, Inc.
Emergent Technologies Corporation
FEP Analytic
Flexible Manufacturing Systems, Inc.
Genus, Inc.
Gryphon Products
Hercules Specialty Chemicals Company
Ion Beam Technologies, Inc.
Ion Implant Services
Isitec Corporation
Lehighton Electronics, Inc.
MacDermid, Inc.
Machine Intelligence Corporation
Machine Technology, Inc.
MG Industries/Scientific Gases
Micrion Corporation
The Micromanipulator Company, Inc.
Micronix Corporation
Oneac Corporation
Pacific Western Systems, Inc.
Peak Systems, Inc.
Probe-Rite, Inc.
Pure Aire Corporation
Sage Enterprises, Inc.
Semi-Gas Systems, Inc.
Silsco, Inc.
The SEMI Group, Inc.
Universal Energy Systems, Inc.
UTI Instruments Company
VLSI Standards, Inc.
XMR, Inc.



Linkages

To maximize the value of cooperative research, the SRC provides mechanisms for discussion and exchange of ideas and information among all participants.

With access to experienced industrial insights from SRC members, university faculty channel creative and innovative research concepts toward useful applications and, in the process, provide a more practical education to graduate students. Industry's reward for involvement in the research process is useful new technology and a larger pool of better-prepared job applicants.

The SRC's linkages that accommodate interactions between industry and the universities, among universities, and among member companies, are described below. As linkage? are strengthened by interest and active involvement, the benefits of cooperation multiply.

Advisory Activities

Technical Advisory Board (TAB)

The Technical Advisory Board, made up ofrepresentatives from each of the member companies, is the SRC's major research advisory group and the prime technical interface to the companies. The TAB is organized into three technical committees: Microstructure Sciences, Design Sciences, and Manufacturing Sciences, corresponding to the organization of the research program. The TAB Executive Committee provides global guidance and coordinates the technical committees' activities. The TAB annually reviews each component of the research program as well as proposals for new funding and examines the continuing relevance, quality, and productivity of each project.

University Advisory Committee (UAC)

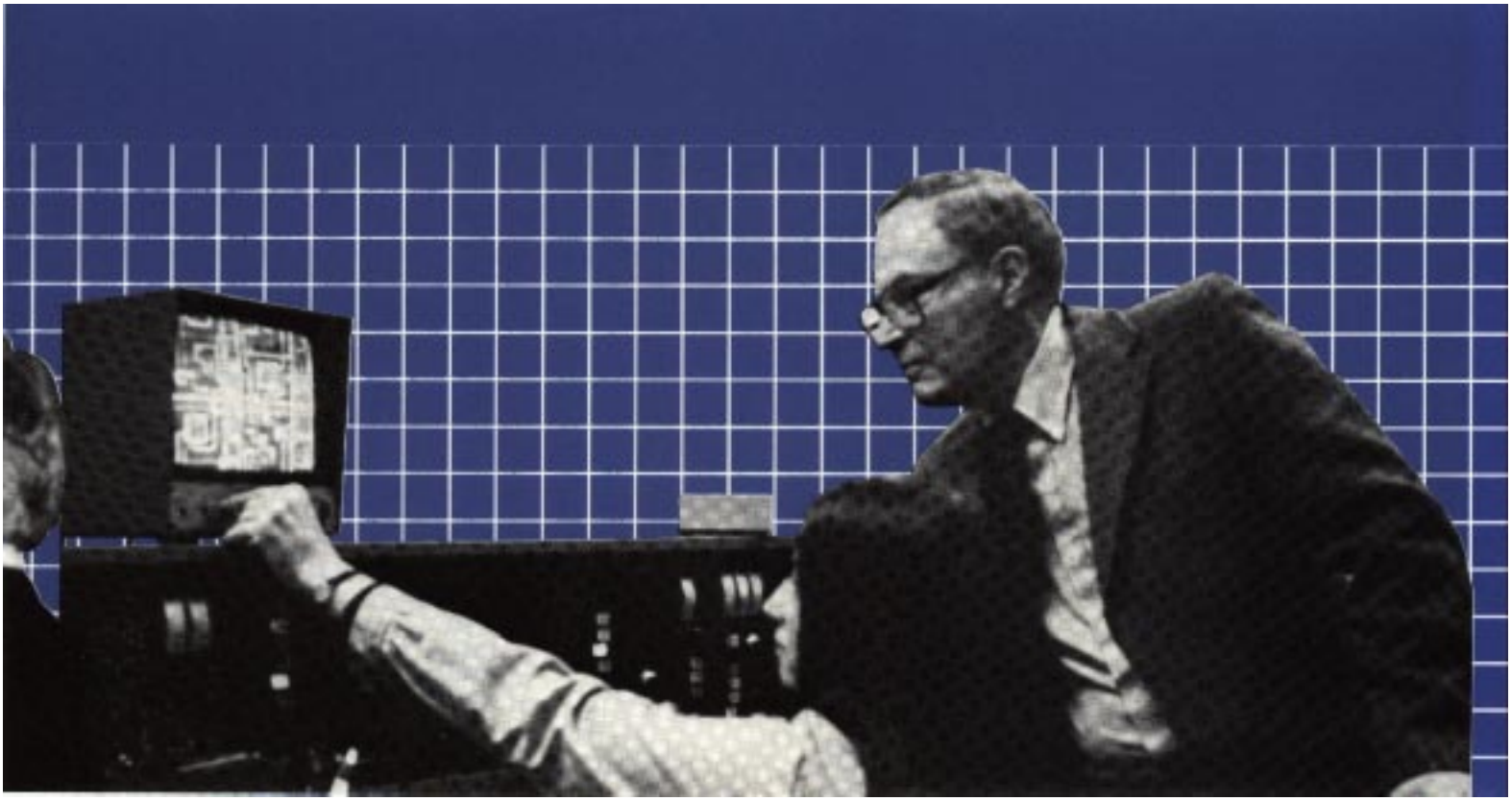
The UAC is an independent body of university faculty that meets twice a year, including an annual meeting with the SRC Board of Directors and TAB, to give counsel on issues relative to the university community. This body has an important role in establishing policy for the research program.

Workshops

Workshops are designed to provide the SRC with a broad perspective on a specific technical area being considered as a research initiative. A Technology Assessment Workshop, held in 1985, provided an evaluation of selected foreign IC technologies relative to their status in the U.S. semiconductor industry. Other 1985 workshops addressed Post-Shrink Silicon Devices, Health and Safety, and In Situ Processing. Workshops on Software Portability and Technology Transfer are planned for 1986.

Industrial Mentors

An Industrial Mentor is a scientist or engineer from a member company who maintains an active constructive interface with an SRC principal investigator. The Industrial Mentor Program was conceived by the Technical Advisory Board and inaugurated by the SRC in 1983 with 42 mentors from 9 companies. Participation has grown to 248 mentors from 32 companies. The mentor advises the investigator on industry knowledge in the subject area, consults on research techniques and directions, and relates results to industry needs. The mentor program is proving to be the single most valuable link between the research and industry.



Technology Transfer Activities

Topical Research Conferences (TRCS) provide an environment for active dialogue among the SRC researchers and industry experts in a specific area. A unique forum for cooperation, these conferences serve as a vehicle for early access to research results, input from unpublished industrial research efforts, and constructive criticism of research efforts. During 1985, TRCs on Placement and Routing, and Quarter-Micron CMOS Technology were held. Each included over 60 participants. Five Topical Research Conferences are planned for 1986.

Technology Transfer Courses (TTCS) provide hands-on experience with a new technology in the university laboratory where it was invented. Particularly in the case of software and analytical techniques, a direct transition can often be made from university research to industrial use. Taught by the university researchers, short courses have proved so popular that each has been over subscribed. The courses taught in 1985 were: FABRICS II; Microstructures Characterization; AIDE 2, An Analog CAD Package; Modeling of Heterojunction GaAs Devices for Circuit Applications; and BSIM (Berkeley Short-Channel IGFET Model). Several of these will be repeated in 1986.

Early Awareness Technical Briefings(EATBs)provide a priority review of a recent invention or breakthrough. These briefings can be important in an industry where timeliness is a major competitive asset. One EATB was held in 1985 at Stanford University to present the multilayer metallization work of Professor Krishna Saraswat. These briefings are scheduled at any time that a worthy event occurs.

Information Dissemination takes a variety of forms in order to serve the diverse needs of SRC members. Information Central is an SRC database that accommodates electronic mail, requests for publications, and event registration for over 250 focal and remote participants. It is supporting an increasing portion of communications within the SRC community. The SRC library now contains over 1500 publications generated from university research and by staff of the SRC that are available to member companies and research investigators. The number of publication requests has risen to over 1000 a month. Most are filled within 48 hours. The monthly SRC Newsletter, which was initiated in July of 1983, reached a circulation of 2600 by the end of 1985. A periodic newsletter, known as SRC IMPACT!, was launched during 1985 to bring items of special achievement to the attention of members of the Board of Directors and TAB.

Industrial Resident Program

The SRC provides the opportunity for member company personnel to join the SRC technical staff forperiods of one to two years. This residency program provides valuable experience in relevant technologies and technology transfer. Working with the SRC staff, the residents provide industry perspective to the research effort and participate in monitoring the research contracts. Having an employee on site for continuous access to the research program is an excellent mechanism for maximizing the benefits of SRC membership.

Fellowship Program

The SRC fellowship program will begin in the fall of 1986 for twenty students seeking advanced degrees in microelectronics. The goal is to increase graduate student support (beyond that already going to graduate students associated with SRC contracts) in the specific areas of microelectronics that are of interest to SRC companies. To ensure relevance, the fellows' research will be directed by SRC investigators.

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Monolithic Memories, Incorporated
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Jim Gordon
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Pallab Chatterjee
Xerox Corporation
David Franco

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E.I. du Pont de Nemours & Company
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GTE Laboratories, incorporated
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Hewlett-Packard Company
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Union Carbide Corporation
William E. Beach
Xerox Corporation
James Vesely

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Varian Associates, Incorporated
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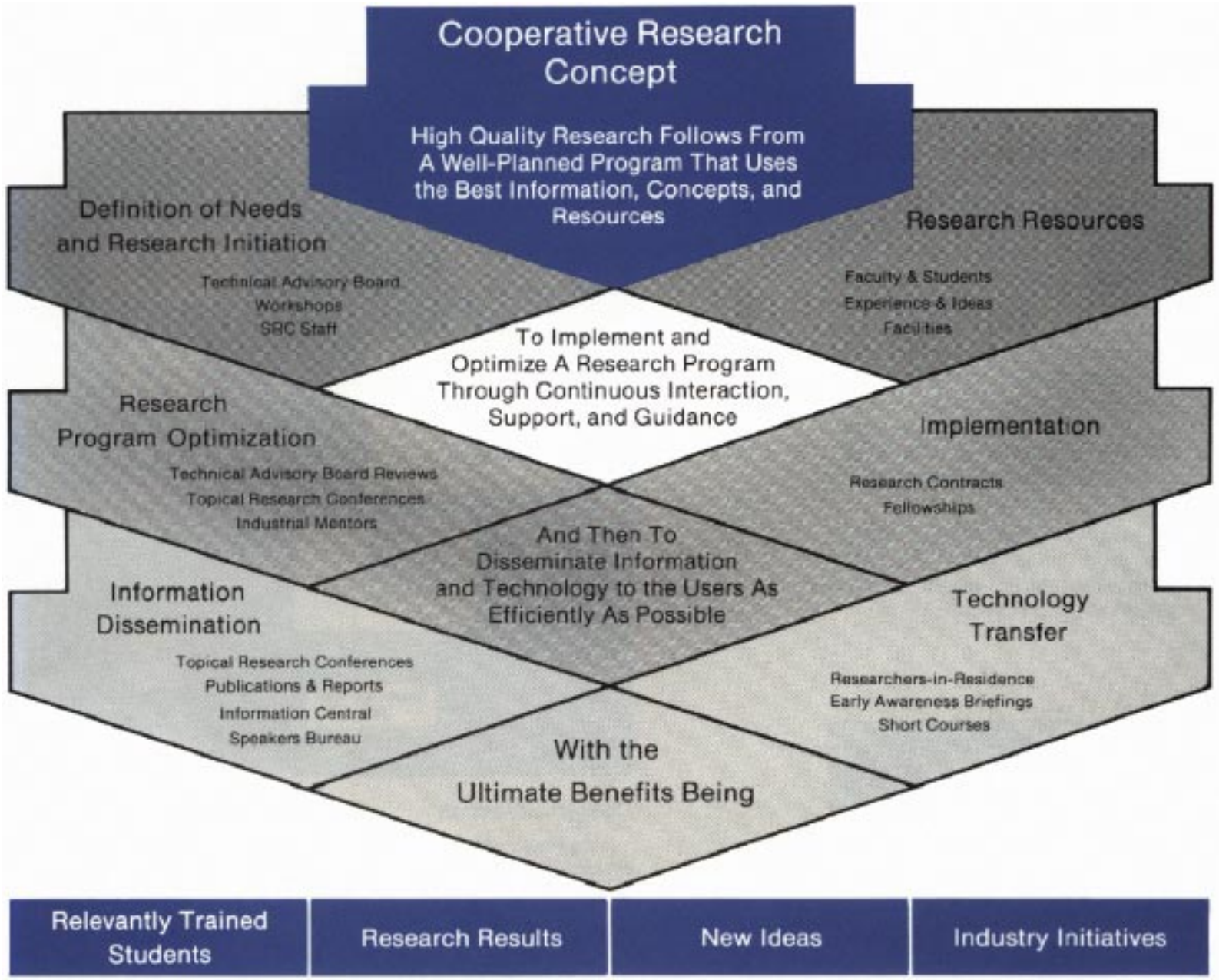
Westinghouse Electric Corporation
Michael Michael



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Massachusetts Technology Park Corporation
Professor Andrew J. Steckl
Rensselaer Polytechnic Institute
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University of Illinois at Urbana-Champaign
Professor Kensall D. Wise
University of Michigan

Introduction

The research program of the SRC is managed as three overlapping areas: Manufacturing Sciences, Design Sciences, and Microstructure Sciences. A total of 43 universities are participating in the performance of over 200 research tasks. Most of these tasks are focused on the defined research goals of the SRC, others are exploring related opportunities. The tasks and goals are being related through programmatic planning documents referred to as roadmaps. Specific research efforts have been selected based on the relevance of the proposed task, the capability of the researchers, and the demonstration of innovative ideas for the research.

Examples of SRC research thrusts are given in the subsequent pages along with selected results from the actual research projects.

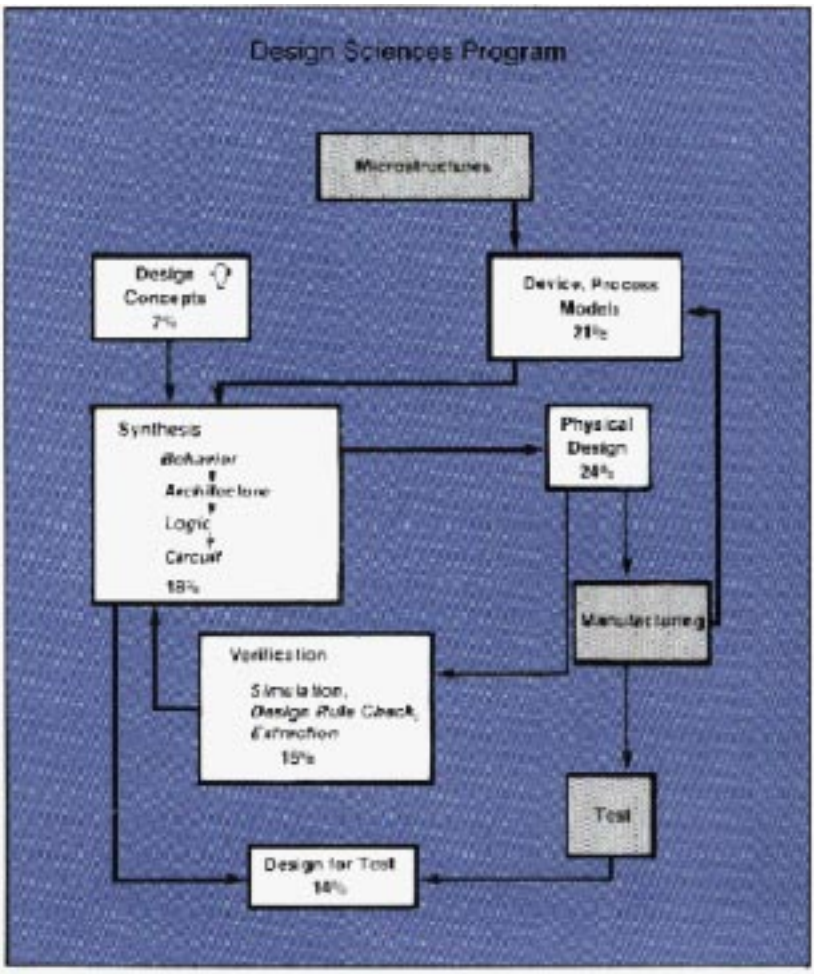
SRC 1994 Global Research Goals

250-fold increase in functionality from 1984.

10^4 increase in performance as measured in gate-hertz/cm^2.

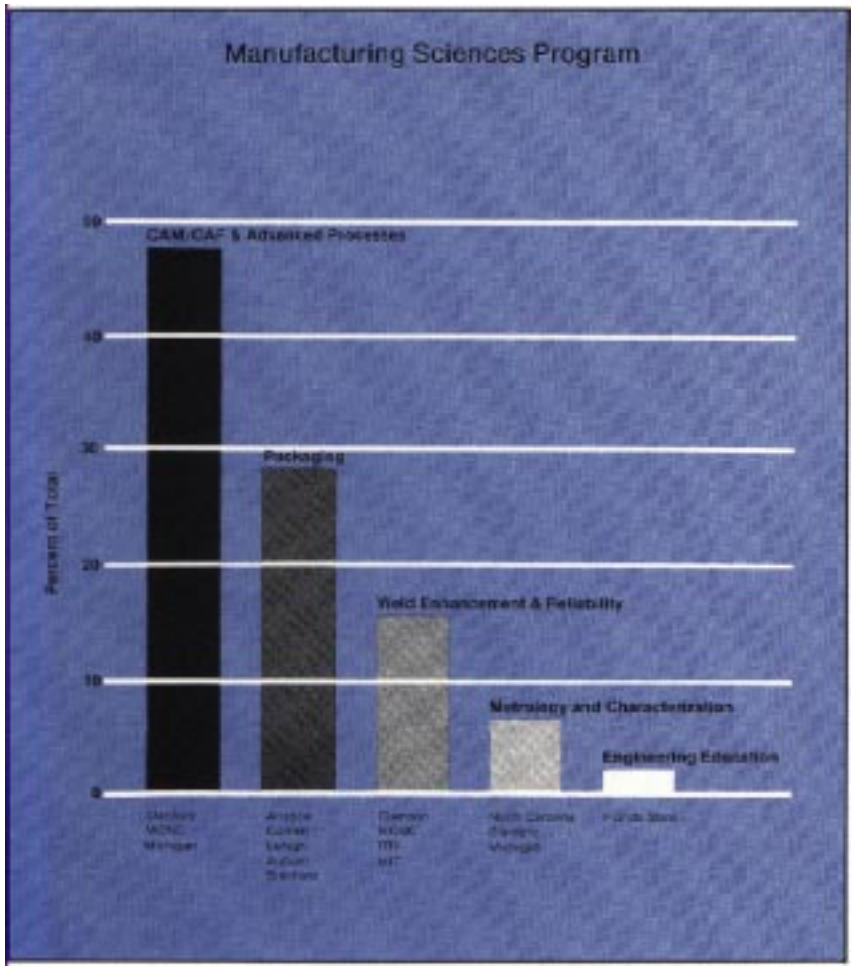
Constant chip reliability of 10 failures in one billion hours.

500-fold reduction in cost/functional element.



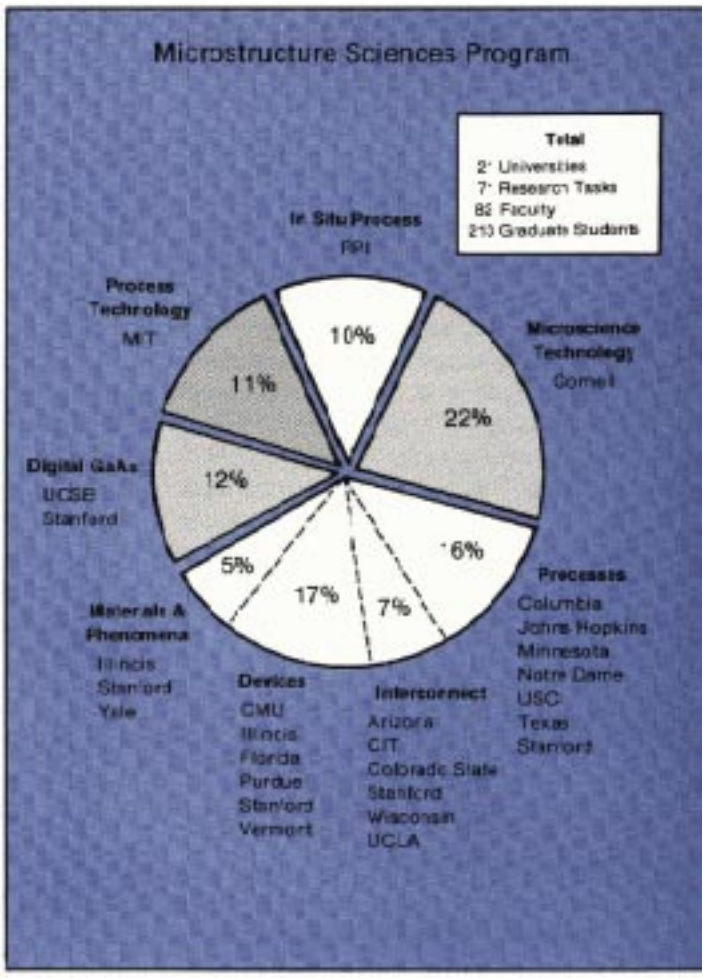
Design Sciences

In the design sciences, goals are focused on the system design environment, design productivity, design for test, reliability, and functional throughput rate. Attention is being given to system partitioning tools, design databases, design for reliability, integration of the test and design environments, a metric for simulation completeness, and performance and power constraints on synthesis. Over 70 percent of the design effort is focused in two centers-of-excellence and a one program.



Manufacturing Sciences

The mission of manufacturing sciences is the quantification, control, and understanding of the semiconductor manufacturing processes necessary to achieve a predictable and profitable product output in the competitive environment of the next decade. This mission includes not only technique research but concern with the image of the manufacturing profession and the caliber of the graduate students that are attracted to the profession. Specifically, research goals are directed to quality, productivity, cost, packaging, CAD/CAM/CAT, and *reliability. Manufacturing sciences research includes efforts that address computer-aided manufacturing and advanced processing technologies, automation, yield enhancement and reliability, packaging, and metrology.*



Microstructure Sciences

Five principal thrusts are being addressed in microstructure sciences: 0.25 micron CMOS in situ processing, gallium arsenide integrated circuits, post-shrink device concepts, and submicron bipolar technology. Each thrust is responsive to the functionality, performance, reliability, cost, device, and process goals that guide the SRC research effort. Proceeding from assessments of present and future device capabilities and needs, these thrusts have been selected to obtain the maximum impact through the next decade from the available university research capabilities and resources.

VLSI Synthesis

The SRC's 1994 design productivity goals can only be met if the design process is moved to progressively higher levels of abstraction. An effort to support design at the behavioral level is underway at Carnegie-Mellon where the development of the Architect's Workbench is being undertaken. This effort is based on the coordinated application of several existing high-level synthesis tools, many of which utilize knowledge-based expert system methods. The goal is to allow the user to experiment with different synthesis approaches and to make estimates of system performance for contemplated designs. A related research effort at Berkeley, involving several faculty and visiting industrial fellows along with a large group of students, is exploring the problem of automatically synthesizing the SPUR Reduced Instruction Set Processor from behavioral level to error-free layout, subject to the constraint that the result must approach the quality of human design. The experiences of this group in attempting to integrate a subset of Berkeley tools and to identify new design tools that are needed to support automatic synthesis will be reported at an SRC Early Awareness Technical Briefing in May, 1986.

Stochastic process models have been developed as a part of the FABRICS effort at Carnegie-Mellon. In broad terms these programs support the efficient modeling and simulation of process response to realistic random disturbances. They also provide statistical estimates of circuit parameter variations and yield projections, and support the tuning of the software to correctly represent existing integrated circuit fabrication systems. During 1985, access to the FABRICS suite was improved by including a graphical process editor, PED, and by the introduction of an incremental process interpreter/compiler called PI/PC. Further work in the FABRICS System is planned in 1986 with the goal of a prototype Microvax II implementation of a Process Designer's Workstation.

If design is to be moved to higher levels of abstraction, then efficient and effective languages are needed to facilitate the description of a design. HOFF is an exploratory language developed at Brown University that fully integrates parallelism and synchronization constraints, supports hierarchical data and module definition, permits designs to be parameterized and specified recursively, and supports a model of computation tailored to VLSI design. A new hierarchical layout methodology, called HELM, has also been developed at Brown to automatically produce layouts from hierarchical descriptions of device topologies and is intended to be used in conjunction with HOFF to provide powerful support for synthesis.

An area of increasing importance is that of analog MOS circuit design. However, virtually no synthesis tools exist in this field. The problem is made more difficult by the fact that device level models for analog synthesis must be much more accurate than those for digital design. In 1985, several SRC research tasks considered various phases of the analog MOS synthesis problem. A prototype CAD package called AIDE2, has been developed at Georgia Tech to support the high-level design of switched capacitor and nonlinear circuits by using a standard, configurable cell.

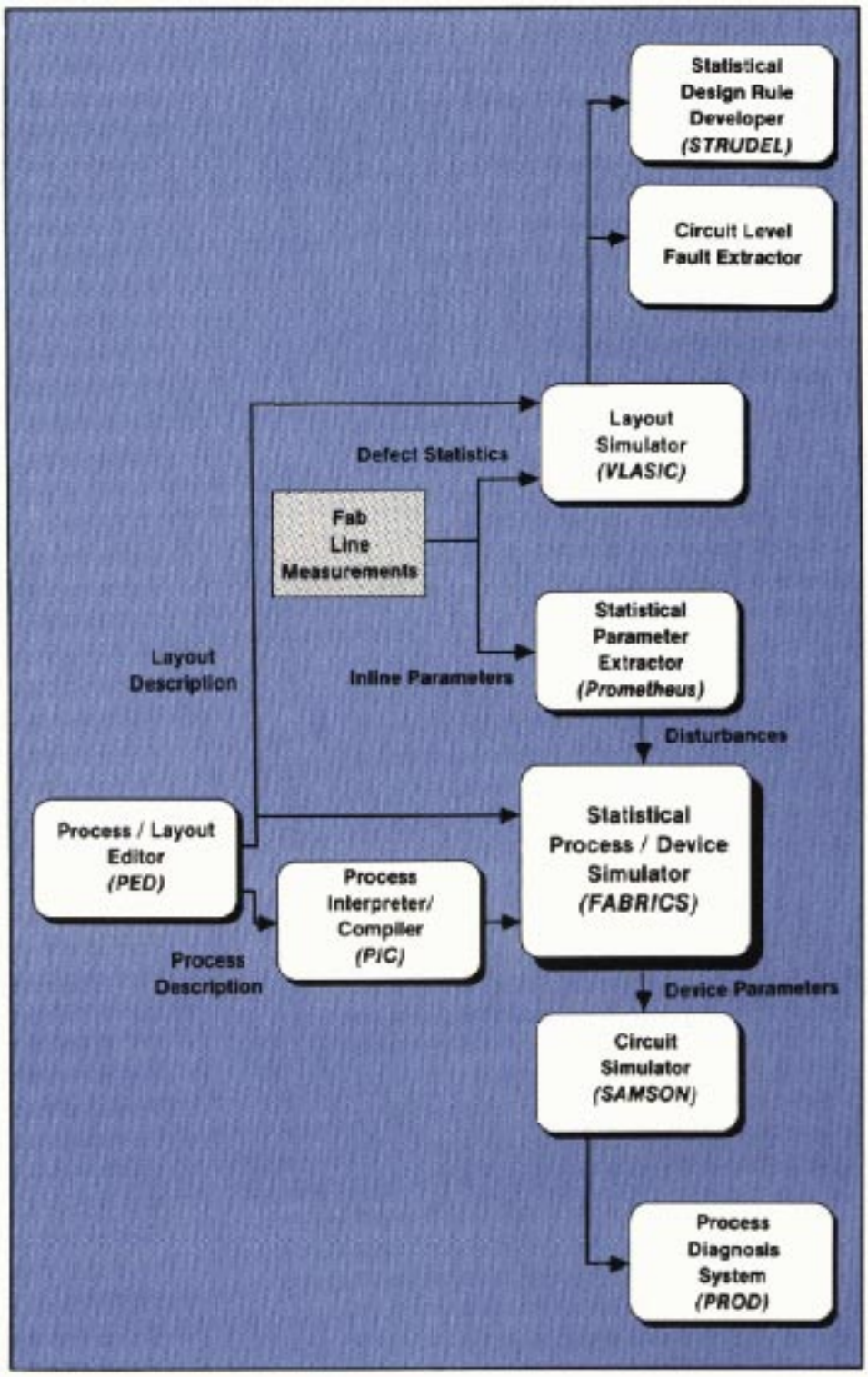
High quality synthesis for analog MOS circuits is often based on the experience of the designer. An effort to apply knowledge-based expert system methods to analog synthesis was undertaken at Carnegie-Mellon, and a prototype program called OASYS has been developed to support analog-to-digital converter design. In an effort to provide analog cells similar to those available in digital design, a task at Berkeley is constructing a scalable cell generator for analog circuits.

The FABRICS System: integrated approach to CAD/CAM/CAT

FABRICS provides the common denominator for minimizing manufacturing cost per chip, concentrating on the parametric variations inherent in the fabrication process and employing efficient numerical and/or analytical models of the fabrication steps used to realize semiconductor devices manufactured in CMOS, NMOS, and bipolar technologies. The accuracy of FABRICS is enhanced by tuning it to a particular fabrication process with the PROMETHEUS statistical parameter extraction program, yielding device parameters that are in close correspondence with those measured under actual manufacturing conditions. FED, allows users to specify processes by defining lithographic masks and process conditions. FABRICS, in combination with a circuit simulator such as SAMSON, may be employed for a number of tasks ranging from design verification/optimization to process diagnosis to statistical process control. PROD, a tool for process diagnosis, uses FABRICS for efficient fault simulation. The VLASIC yield simulator can be used for prediction of the decrease in yield due to spot defects (shorts or breaks caused by local lithographic errors). The STRUDEL statistical design rule developer derives layout rules that maximize total yield in the design of IC circuits. CMU's goal is an overall CAD program that takes full advantage of constantly evolving technology by providing IC designers and test engineers with statistical process characterization. Information gathered in the IC design stage subsequently becomes effective for statistical process control purposes.

SRC Contract 82-11-007
Carnegie-Mellon University

Professor S.W. Director,
Director, Center of Excellence



CMOS Technology

The advantages of CMOS relative to alternative technologies make it the technology of choice for high complexity ULSI circuits. To aid in accomplishing the industry-established 1994 goals and objectives of the SRC, a major research thrust in 0.25 micrometer CMOS technology is underway. The primary objective of the research is to develop a low power, high performance device/circuit and fabrication technology at the practical scaling limit of MOSFETs. Hence, the key technology and knowledge issues required to scale 1 micrometer minimum-feature-size (MFS) design rules downward are being addressed. This requires research in materials processing, thin film deposition, lithography, etching, device and circuit modeling, and characterization directed to obtaining the appropriate device elements: isolation, wells, gate structure, contacts, and interconnect levels. Each element, and integration of the elements, provides a set of problems to be solved.

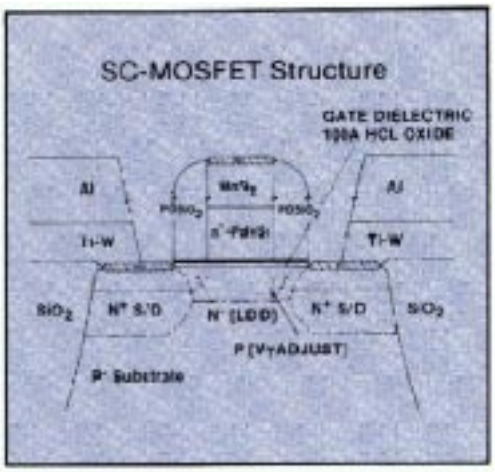
The SRC's 1994 complexity goal translates into a functionality equivalent of a 256 Mbit DRAM. This has been shown to be an aggressive and appropriate goal based upon the projection of present technology. The SRC's goals can be described in terms of a density of 20E6 transistors/cm^2, a process feature size of 0.25 micrometers with layer thicknesses of 10 nanometers, an overlay accuracy of 25% of the feature size, 4 levels of interconnect, 50 picosecond propagation delay time, 5 femtojoule/gate power dissipation, and an analog/digital capability of 16 bit accuracy at 100 megahertz.

In support of this thrust, the SRC has an established Center-of-Excellence at Cornell University which is directed towards fabrication of 0.25 micrometer MFS microstructures for integrated circuits, an Advanced Process Technology program at MIT, and individual projects/tasks at Berkeley, Carnegie-Mellon, Clemson, Colorado State, Columbia, Illinois, MCNC, Minnesota, NC State/Research Triangle Institute, RPI, Southern California, Stanford, Texas, Vermont, Wisconsin, and Yale. Research vehicles are defined as (1) a 6-transistor cell, 1k SRAM array of equivalent circuit density equal to a 4 Mbit SRAM, and (2) a 16-bit, 10 MHz A/D converter.

Hot carrier degradation is a key problem for submicron MOS devices. To better understand this, a technique has been developed to study the charge transfer in individual interface/trap states that produces low frequency telegraph noise signals. Fundamental charge transport and defect generation mechanisms that limit endurance of micron and submicron devices are being identified. Techniques have been developed to use simulations to optimize doping profiles for highly stressed devices.

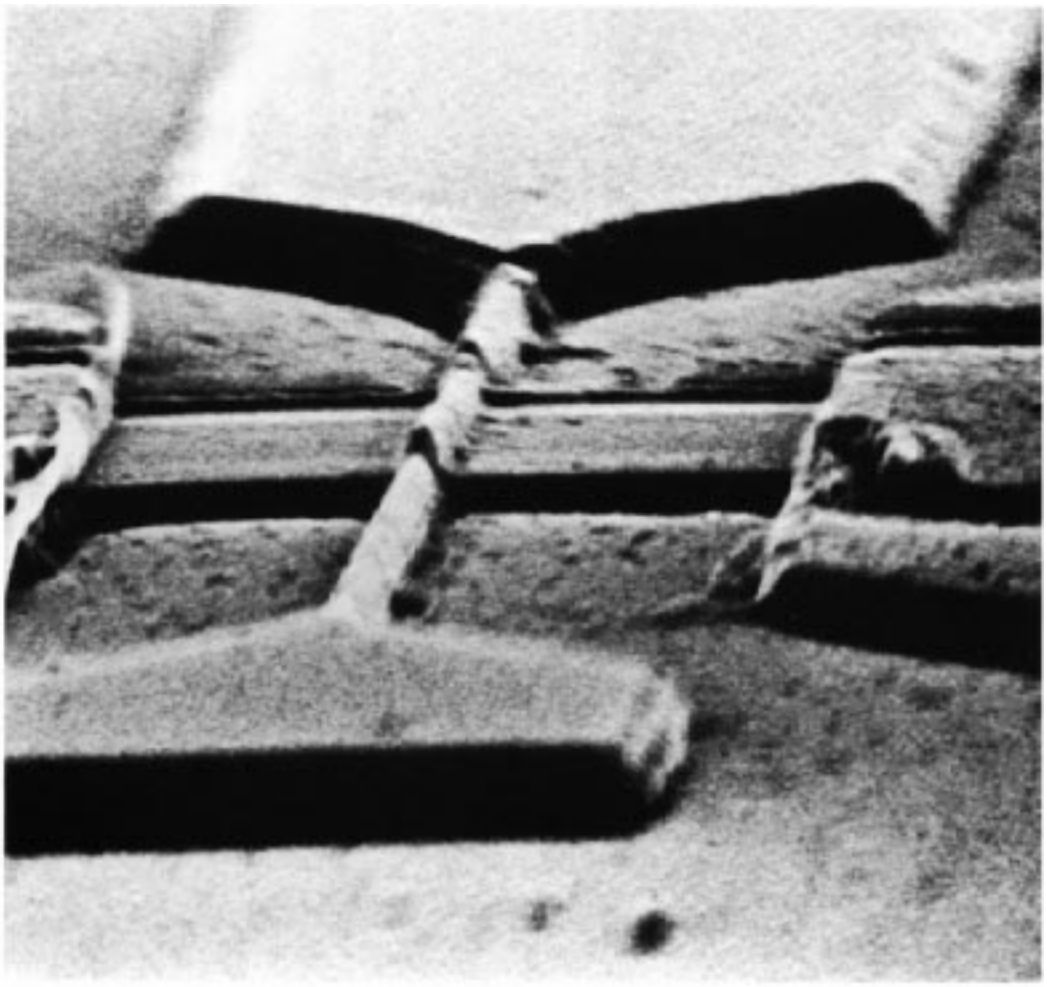
Rapid thermal processing (RTP) is being applied to fabrication of high quality 100 angstrom silicon oxides and nitrided silicon oxides. Thicknesses of several hundred angstroms take only a few minutes to grow.

An ion implantation technique to inhibit lateral silicide growth has been developed. Study of $TiSi_2$ is developing relationships between resistivity and structure, chemistry, and morphology.



Cross-sectional diagram of NMOS device shown in the photograph: modified LOCOS isolation, 10 nm gate dielectric produced by RTP; E-beam direct-write pattern transfer for gate formation; LDD extensions, silicided gate, source, and drain regions; source/drain junction depths of 0.15 micrometer: and TiW/Al metallization.

Fully self-aligned, surface channel quarter-micron NMOS device.



Quarter-Micron Transistor

A principal SRC thrust is the fabrication, simulation, and characterization of quarter-micron, minimum-feature-size microstructures for CMOS ICs. Extensive research is ongoing to enhance and characterize the present NMOS technology, and to implement a corresponding PMOS technology. Characterization of all aspects of the quarter-micron technology is essential, using TEM, STEM, HRTEM, SEM, SAM, RBS, SIMS, I-V, C-V, G-V, EDS, and EELS facilities.

SRC Contract 82-11-001
Cornell University

Professor Noel C. MacDonald,
Director, Center of Excellence

Shallow junctions, <0.15 micrometers, that are required to avoid short-channel effects, can be achieved if temperatures are kept below 900°C, or if RTP or excimer laser processing is used. Germanium can be used to pre-amorphize the silicon for ion implantation and reduce the rapid initial diffusion of the implant tail.

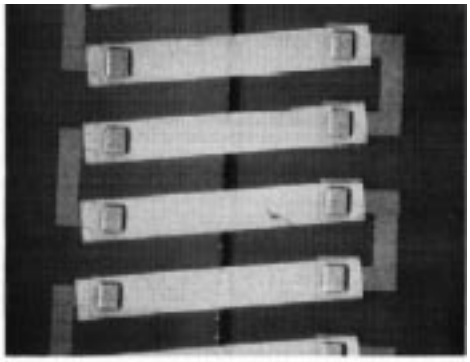
The use of selective deposition of tungsten for gate, source, and drain conductivity enhancement; unframed contact etch stops; metallization barriers; contact openings; or via filling for planarization looks very promising. Advantages are low resistivity, high electromigration resistance, low contact resistance, a thermal expansion close to that of Si, and selective deposition in a hot-wall, low-pressure (250 millitorr) CVD reactor at 300°C.

It has been shown that layering silicon-doped aluminum with titanium can significantly reduce electromigration by as much as 15 times the results achieved with the standard metal interconnection. An SRC Early Awareness Technical Briefing (EATB) was held to transfer the results of this layered-film interconnection technology to the SRC industrial community.

Packaging

The knowledge base for integrated circuit packaging has traditionally been in the material sciences since it has been basically a polymer, metal, and ceramic fabrication art. With the development of more complex, larger, and higher performance integrated circuits, it has become apparent that the thermal, electrical, and mechanical parameters of the package are becoming increasingly important factors. For the SRC, industry input has defined packaging sciences as an important area of research because of both the performance and cost requirements associated with future complex chips.

IC packaging research focuses on the advanced technologies for future use in both first- and second-level packaging systems. Areas needing technological understanding and enhancement include: IC interconnect and attachment techniques; new protective techniques (nonhermetic/ hermetic package); additional thermal management concepts; mechanical stress analysis; computer-aided modeling and simulation techniques (including know/edge base); thermal, stress, and electrical parameter analysis; new secondary substrate materials; and interconnect systems. To address these needs, SRC packaging research is underway at Arizona, Auburn, Cornell, Lehigh, and Stanford Universities. New electrical and thermal models are being developed for packaging applications; a concept in which silicon ICs are mounted and interconnected on a silicon substrate is being pursued; innovative thermal transfer and chip hold-down techniques have been demonstrated; and optical interconnect, both inter- and intra-chip, are being experimentally evaluated.



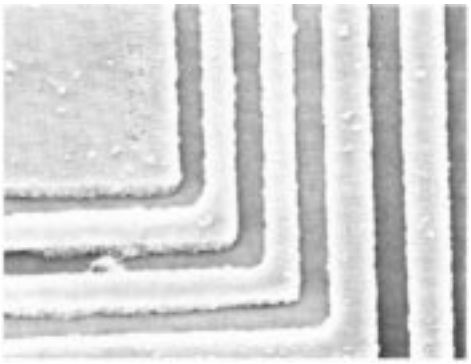
The chip and wafer following interconnection with a second level of aluminum. This closeup view shows coverage of gap by aluminum links over polyimide interlevel dielectric.

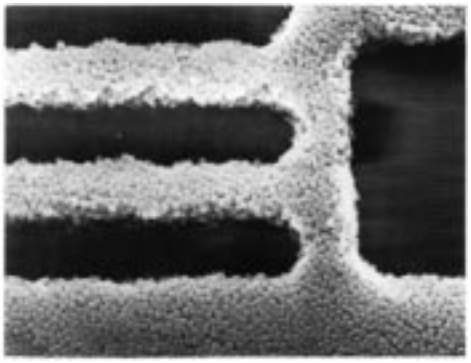
Active Silicon Hybrid Wafer-Scale Packaging Technology

The need for wafer-scale integration to provide a high level of dense interconnection between integratedcircuit functions will continue to grow as system performance becomes increasingly limited by the connections between chips. A silicon-based, hybrid, wafer-scale packaging technology, which circumvents the yield and discretionary interconnect problems normally associated with wafer-scale integration, is being explored. In this approach, pretested integrated circuit chips are mounted in holes in silicon wafers and then interconnected using a standardmonolithic two-level metallization process. The silicon wafer supports the chips and provides a medium for metallic interconnections. MOS and bipolar integrated circuits, fabricated using various processes, may be mixed together in a wafer-scale package combining the flexibility of hybrid ICs with the reliability of monolithic interconnections. A computer program is used to automatically generate pattern data for the via and link masks based on measured values of offset and rotation for each chip.

SRC Contract 84-11-052
Auburn University

Professor Richard C. Jaeger,
Princpal Investigator





The photomicrographs show thin lines of 0.5 micrometer spherical silicon dioxide particles.

Ceramic Packaging Technology

Advances in integrated circuit packaging technology are key to the system implementation of ULSI circuits. In ceramics technology, the major unknowns, both theoretically andexperimentally, are related to shrinkage control with tolerances 1-to-2 orders of magnitude beyond the state-of-the-art and fine-line structures, capable of 5 micrometer line width conductor and/or insulator patterns. Two significant milestones have been accomplished: (1) the deposition and sintering of particulate ceramic films with no lateral shrinkage and (2) the development of lithographic processes to create features in the particulate films which have arbitrary shape and have dimensions as fine as 5 micrometers.

SRC Contract 83-01-033
Massachusetts Institute of Technology

Professor L. Rafael Reif,
Program Director

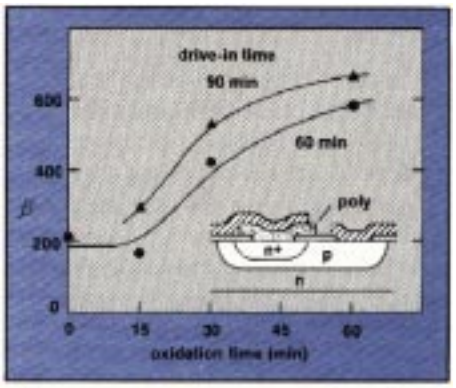
Bipolar Technology

In response to the interests of its members, the SRC is creating a research effort in bipolar technology in order to provide a knowledge base for higher performance bipolar integrated circuits. Fundamentally, it appears that bipolar device performance can be enhanced at smaller geometries without the detrimental effects that limit submicron MOS device performance. Bipolar device applications, centered on their high speed capabilities, are expected to continue their major role in high speed computers based, in part, on recent advances in packaging technology.

Major goals in advancing the state-of-the-art of bipolar technology are utilization of polysilicon emitters, application of trench isolation, efficient thermal management, and improvement in models for better and more accurate circuit simulation. These enhancements will increase the speed of bipolar circuits, improve density, and maintain their superiority for high performance mainframe computer applications.

The SRC has contracts with Carnegie-Mellon University, Purdue University, and the University of Florida for research work on polysilicon in bipolar structures and the interfacial barrier layer between the polysilicon and the single crystal substrate, on solid phase epitaxy, and on models and measurement techniques for bipolar IC structures.

Results have shown that increasing the thickness of the interfacial layer increases the gain of the device while introducing variability in device behavior. Removal of the interfacial layer can lead to epitaxial growth which can occur at reduced processing temperature. Presently, modeling is focused on inclusion of basic physical concepts in the device models. Predominant high current effects have been identified and key simplifying assumptions are being made to facilitate the implementation of physics into the circuit model. Analytical expressions for the position dependence of excess minority carriers in the heavily doped emitter region have been developed. A general method for incorporating charge-based device models into SPICE2 has been defined using "User Defined Controlled Sources."



Results from one run of wafers. The current gain (beta) is observed to increase with the oxidation time for oxidation times greater than 15 minutes. The oxides were grown in the LPCVD reactor at 625°C just prior to polysilicon deposition. Inset: structure of the polysilicon emitter transistor.

Polysilicon in Bipolar Devices

It has long been recognized that the interfacial layer between the polysilicon and the single crystal emitter has an important effect on bipolar transistor gain. Transistors are being fabricated in which the thickness of the interfacial layer is controlled by varying the length of a thermal oxidation prior to polysilicon deposition. The oxides are grown in the liquid phase chemical vapor deposition (LPCVD) system just prior to polysilicon deposition, which should result in a cleaner and more reproducible interface. Data compiled so far suggest that the device characteristics are slightly dependent on the oxidation time, provided the oxidation time is less than 15 minutes. The implication is that polysilicon emitter devices are relatively tolerant to oxygen exposure prior to loading in the LPCVD system. Future investigations will include confirmation of these data and studies of transistors with longer oxidation times.

SRC Contract 83-01-011
Carnegie-Mellon University

Professor David W. Greve,
Principal Investigator

Physical Design

The term 'physical design' usually refers to the placement and interconnection of rectilinear blocks on the surface of an IC chip. The physical design problem is extremely important since it directly impacts manufacturing yield by determining the required chip surface area and because resulting interconnection lengths impact circuit performance. Many of the problems in physical design are complex in that their solution complexity is not simply related to the problem size. This has given rise to a search for efficient heuristic algorithms and progress can be reported from the SRC research program during 1985. The software suite, BBL.2, and the layout package, MAGIC, both from the University of California at Berkeley and both partly supported by the SRC, were released to industry for evaluation. The standard cell placement and routing system, Thunderbird, was also completed at Berkeley.

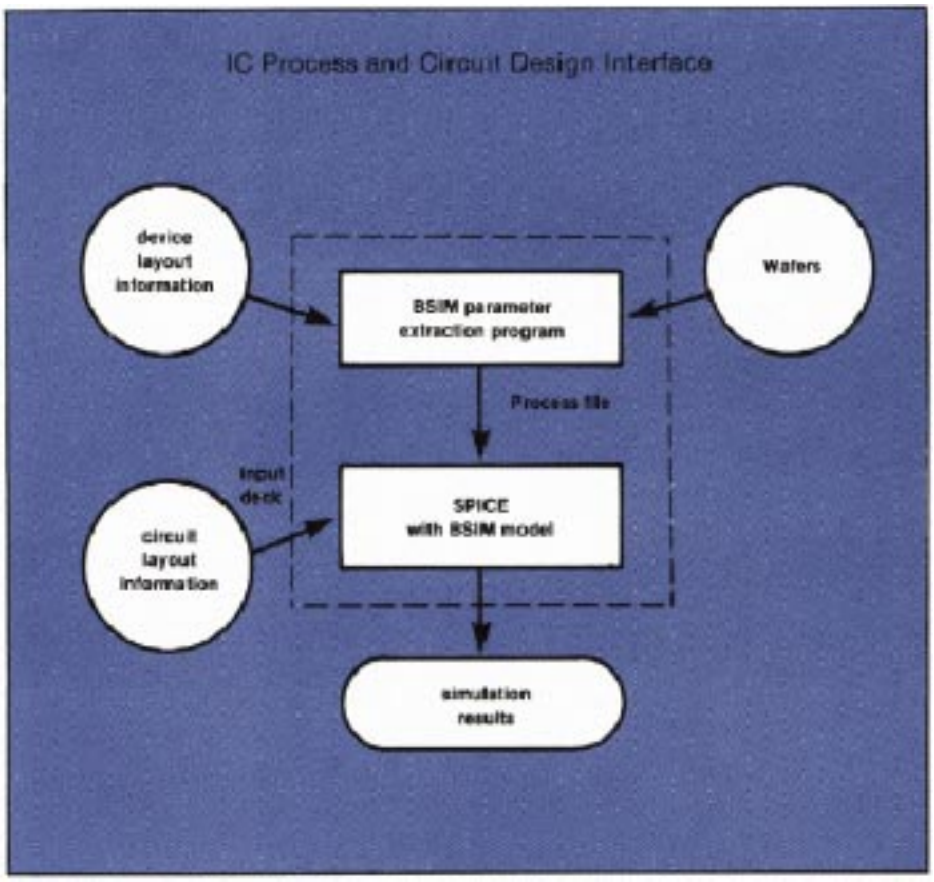
New algorithms for physical design are being sought. The simulated annealing paradigm, whose rationale is based on the random physical phenomena that occur when a material is cooled according to a prescribed schedule, can be shown to converge for certain classes of global optimization problems. The practical problem is that extensive amounts of computing time are required to obtain high quality results. The encouraging factor is that good quality layouts are often obtained as a consequence of this investment. Since simulated annealing is computationally intensive, it offers opportunities for parallel computation. Preliminary studies at both Carnegie-Mellon and Berkeley indicate that substantial performance gains are possible.

BSIM, An IC Process-Oriented Family of MOSFET Models for Circuit Simulation

BSIM (Berkeley Short-Channel IGFET Model) is a family of new MOS device models in SPICE designed to address the need for an efficient computer-aided link between technology and circuit simulation. A process-oriented approach has been established for BSIM that allows rapid model development; only the approximated physics are incorporated, while most process-sensitive parameters are determined empirically. This approach also provides the additional benefits of producing models that are most computationally efficient, are more tuned for automated model parameter extraction, and have better accuracy than existing models in SPICE. BSIM 1 was developed primarily with digital circuit emphasis. In response to a growing need for accurate analog circuit simulation that requires a better model for the output conductance, investigators are working to improve BSIM 1 in this area; and updating will continue in response to feedback from industrial users. Other ongoing projects are related to RSIM 2, an enhanced version for submicron MOSFETs: a new drain-current model with ultimate quarter-micron capabilities, a small-geometry intrinsic device capacitance model crucial for the design of future generations of high-speed circuits, and a hot-electron substrate current model that wit/assist circuit designers in identifying possible hot-electron reliability problems early in the design stage.

SRC Contract 82-11-008
University of California at Berkeley

Professor Donald O. Pederson,
Director, Center of Excellence



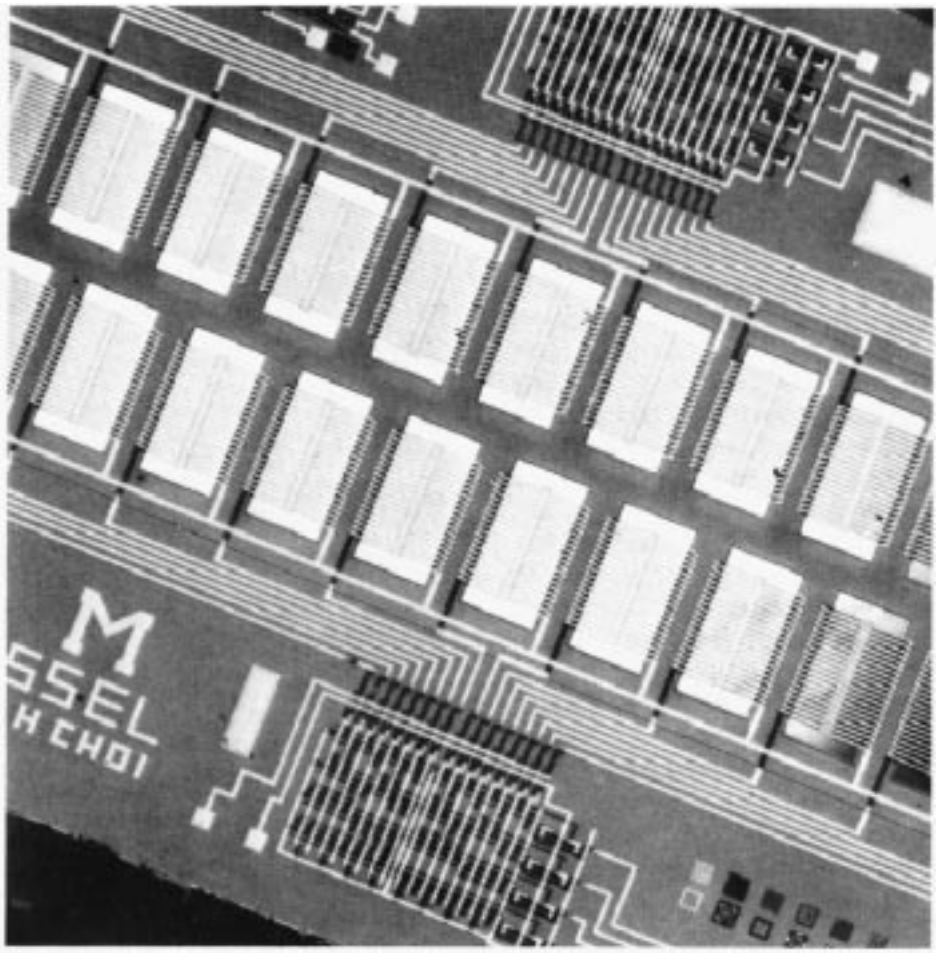
Manufacturing Research:

CAM— Computer-Aided Manufacturing
CAF— Computer-Aided Fabrication
CIM— Computer-Integrated Manufacturing
CAT— Computer-Aided Test

In the research agenda of the SRC, manufacturing productivity and quality have been given high priority. Historically, little effort has been invested by U.S. universities in semiconductor manufacturing research. For this SRC initiative the research scope has been defined, the attention of competent investigators has been obtained, and a credible research program is underway.

Manufacturing sciences must progress at a rapid pace in the U.S. Neither the tools nor production know-how required to produce competitive mega-device chips is available. Advances are required in simulation of the equipments and processes, in the control of the integrated fabrication sequence, in automation, in process monitoring and control, in testing, and in providing strong interfaces between the manufacturing and design environments.

Manufacturing science and technology research is being carried out at Stanford (CIM/CAF), the Microelectronics Center of North Carolina (CMOS Fabrication Research), and the University of Michigan (Expert Systems, Sensors, and Machine Vision). Results to date include demonstration of in-process sensors, such as a thermal imager for temperature profiling and an end-point detector for plasma etching. Research is underway to develop a manufacturing simulation environment that includes models for processes (reactive ion etching), equipment, and material flow.



In-Process Thermal Sensor

The development of improved sensors for monitoring semiconductor processes in situ represents one of the key needs of automated process facilities. Research in integrated sensors has resulted in the development of a silicon 32-element infrared/thermal imager for use in automated manufacturing. The device consists of a series of dielectric windows in a silicon wafer. Each window supports a thermocouple array that converts incident radiative energy into an electrical output voltage. The device operates over a broad range of ambient temperature, responds to radiation over a wide spectral band, and has a dynamic range spanning seven orders of magnitude. With windows giving an effective linear spatial resolution of 200 micrometers, the chip can detect temperature rises of less than 0.1°C and measures 11 mm x 5.5 mm. On-chip circuitry provides multiplexing and array compensation. The chip is being explored for applications in thermography and laser spectroscopy in connection with in-process and in situ reactive ion etching and chemical vapor deposition.

SRC Contract 84-01-045
University of Michigan

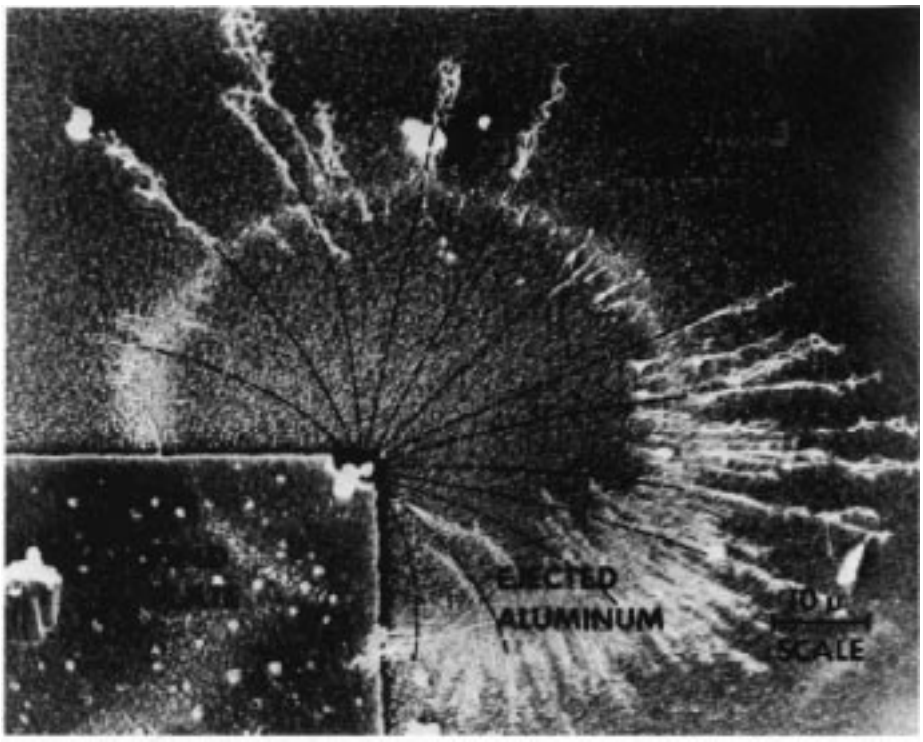
Professor K.D. Wise,
Program Director

Reliability

Reliability is defined as the ability of a system to function as designed under stated conditions for its planned life span. As the complexity of a system increases, a high reliability becomes more difficult to achieve without improving the fabrication technology or design. Integrated circuit technology has been highly successful in maintaining the reliability of an individual chip at an approximately constant level while the chip complexity has increased by many orders of magnitude. Failures are caused by external stresses from the environment (such as high temperature, shock, radiation, or electrostatic discharge) or by changes in the structure induced by packaging defects, diffusion, and drift of charges or atoms under stress. The occurrence of failures is directly related to design margins and the preciseness with which design parameters are achieved in fabrication. The reliability research of the SRC encompasses design, testing, failure mechanisms, and fabrication technology.

The goal of the SRC by 1994 is to achieve a reliability level of 10 failures in one billion hours without burn-in. Burn-in is the technique of exercising the system under stress conditions, prior to delivery, in order to eliminate or minimize the weak members that are prone to failure early in the life of the system.

At Clemson University, an SRC study is underway to examine factors that determine reliability of ICs made with submicron design rules. Additional efforts are being conducted at Illinois, Carnegie-Mellon, Vermont, Cornell, and Stanford in specific areas. This research includes studies on electromigration, electrostatic discharge and charge injection; on intrinsic stability of the oxide silicon system with respect to charge redistribution; on the effects of design on reliability; and on chip coating materials.



The deposition pattern that occurs when a square test capacitor is subjected to a controlled pulse of 75 ns duration sufficient to cause immediate breakdown.

VLSI Reliability: Electrostatic Discharge (ESD) Effects

Electrostatic discharge/electrical overstress phenomena represent a major cause of failure in VLSI components after manufacture. Preventive approaches involve avoiding overstress through proper grounding and use of anti-static work surfaces, and minimizing the effect of overstress through on-chip input protection circuits. A unique time domain reflectometry method for introducing and analyzing controlled amounts of overstress to test structures is being used. Curved trajectories in the deposition pattern of the accompanying photograph indicate that the charged liquid metal moved under the influence of electric 75 ns was required for the combined processes of breakdown, thermal generation, and ballistic transport. This is the first experimental evidence of such a short thermal time constant being associated with the ESD breakdown process. Further examination of trajectory shapes as a function of variables such as pulse width, pulse energy, and device geometry will permit the quantification of thermal time constants and provide information for use in the design of improved protective circuitry and in the study of latent defects.

SRC Contract 83-07-042
Clemson University

Professor Jay W. Lathrop,
Program D/rector

New Device Concepts

In addition to addressing the defined goals of the SRC, research is undertaken to explore future promising areas. This includes quantum domain and gallium arsenide devices that have the potential for extending beyond the present and forecast capabilities of conventional silicon devices as they approach their limits.

The limit of conventional MOSFET silicon technology, based on "shrinking" the layout rules, is generally believed to be in the neighborhood of 0.25 micrometer minimum feature size. However, technology permits the fabrication of artificial structures with dimensions smaller than this, structures whose principles of operation are based on quantum domain phenomena. Devices using such phenomena are ex*pected to exhibit system performance and complexity several orders of magnitude greater than that which can be provided with MOSFET silicon technology. Significant areas of research relate to the fabrication technology, investigation of promising material systems, quantum domain transport and device phenomena, and coupled device systems.*

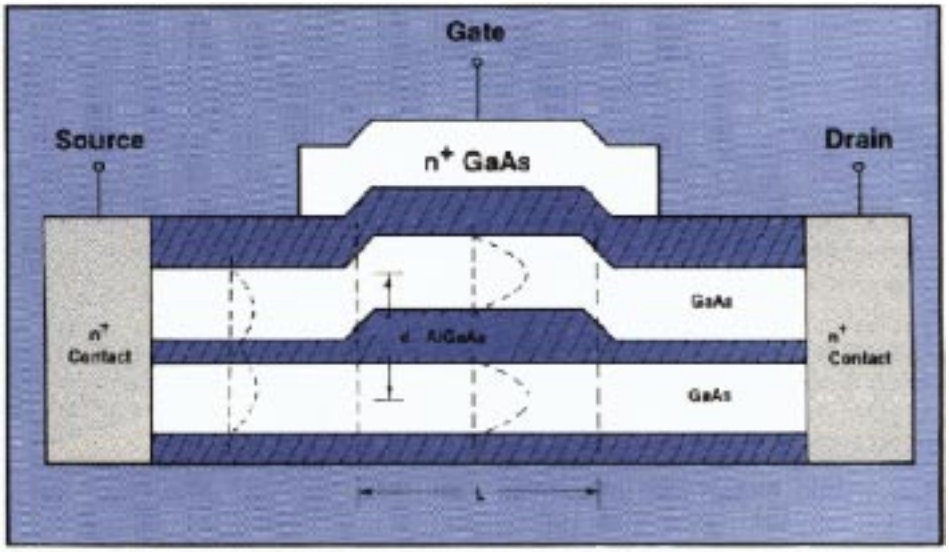
SRC research projects in quantum domain devices include theoretical research on periodic superlattice structures at Cornell, fabrication of two-dimensional electron gas HEMT structures in gallium arsenide at Santa Barbara and Stanford, investigation of superlattices of cobalt silicide and silicon at UCLA and the California Institute of Technology and analysis of quantum transport phenomena at Purdue.

Aharonov-Bohm Device Technology

Novel devices, based on quantum principles and potentially useful for logic and memory elements in integrated circuits at densities greater than those projected to be achievable at the limit of classical scaling theory for conventional MOSFETs, are being investigated. Such devices generally involve either tunneling phenomena or phase shift control of the wave function. A device, based on quantum wave phase interference that occurs between currents flowing in two parallel channels formed by contiguous GaAs quantum wells, has been proposed. Preliminary experiments with a simple structure show oscillations in the conductance as a function of the imposed magnetic field with a period of h/e, indicating an Aharonov-Bohm effect. These devices are expected to have an exceptionally high transconductance and a power-delay product several orders of magnitude smaller than conventional devices.

SRC Contract 83-01-001
Purdue University

Professor Mark S. Lundstrom,
Principal Investigator

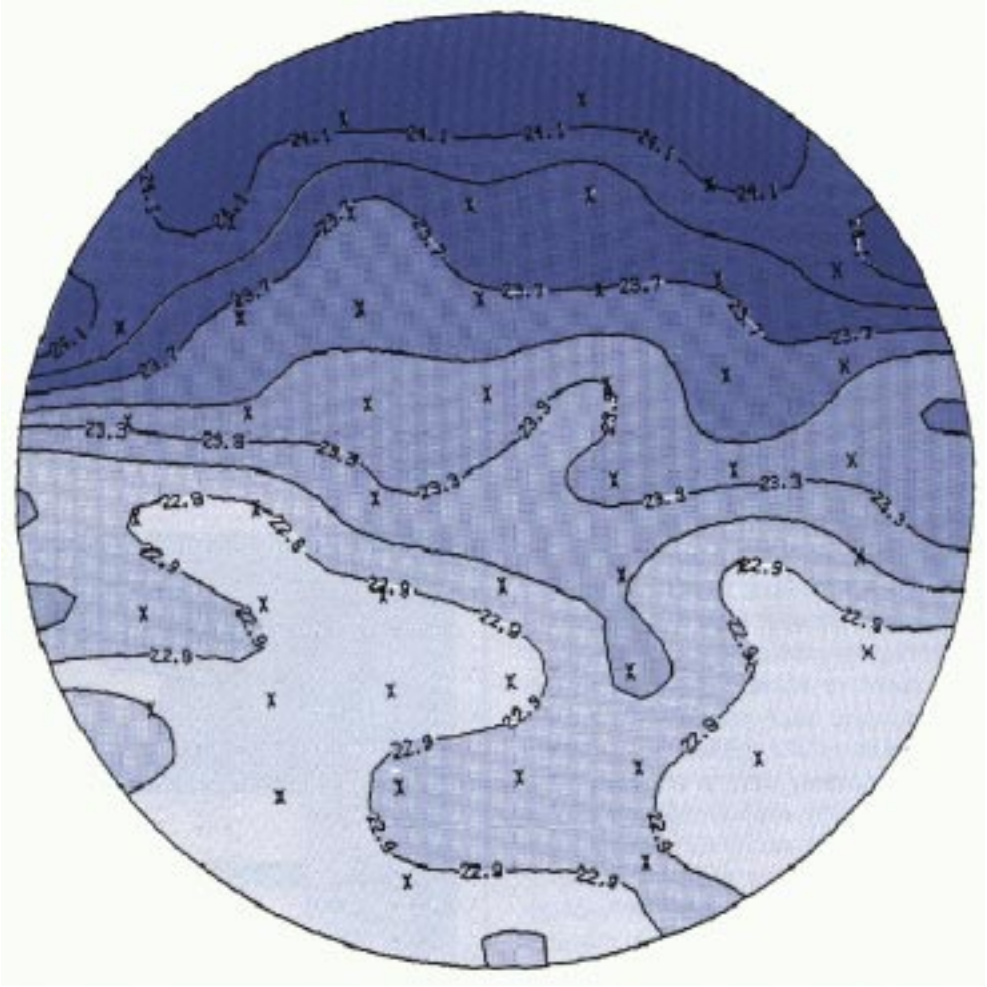


VLSI Design Environments

The 'design environment' presented to the integrated circuit designer is an important factor in determining designer productivity. The quality of the design environment is characterized by the richness of the available too/ set and design libraries, the ease of communication between tools, support for tool installation, and real-time performance of the tools.

In 1985, several SRC research projects explored means to improve the VLSI design environment. The ULYSSES project at Carnegie-Mellon provides expert advice to the designer on too/ selection and coordinates data exchange between the selected tools. It facilitates the use of new CAD tools and has a 'blackboard' architecture with a global data base that allows communication among various expert programs and CAD tools. Currently, ULYSSES is being tested in a hierarchical layout synthesis application in which it controls TALIB, a cell layout program; WEAVER, a routing program; and MASON, a floor planning program.

A second design environment research effort at Carnegie-Mellon explores the premise that natural language interaction with CAD tools can reduce both the /earning time and the activation time for the too/. An experimental natural language program called CLEOPATRA has been developed for circuit simulation post-processing. CLEOPATRA accepts natural language requests from the user for information on simulation results and is able to understand grammatically incomplete questions (e.g., 'headless' relative clauses, abbreviations, etc.). It also supports prefix and infix arithmetic functions, and responds to requests referring to past queries. In 1985, the response time of this interface system was dramatically improved and certain capabilities, such as remembering questions asked and answered in the past session, were added.



A parametric contour map for a processed silicon wafer. This map was produced by an analysis program STAT2 developed by the United States Bureau of Standards, one of the many tools which will be accessible from within Cameo.

CAMEO: An Expert System for Process Design and Personnel Training

An experimental computer-aided design (CAD) system, called Cameo, assists engineers in the specification and improvement of VLSI photolithographic processes. Cameo embodies knowledge in the form of heuristics, tabular data, analytical functions, andprocess simulators. It overcomes some limitations of previous expert CAD systems by providing a highly interactive user interface to the knowledge base, inference engine, and a database describing processes and equipment. Users may choose to engage or bypass any of its expert capabilities, thus making Cameo anything from a VLSI process simulator front end to an intelligent process design assistant and training aid. Among the innovations embodied in Cameo are a highly modular knowledge base containing knowledge for all levels of the synthesis process, support for parallel development of design alternatives in an efficient manner, and finks to existing design and analysis tools such as VLSI process simulators and parametric festers. A second generation version of Cameo with additional features is under development.

SRC Contract 82-11-008
University of California at Berkeley

Professor Donald O. Pederson,
Director, Center of Excellence

In Situ Fabrication

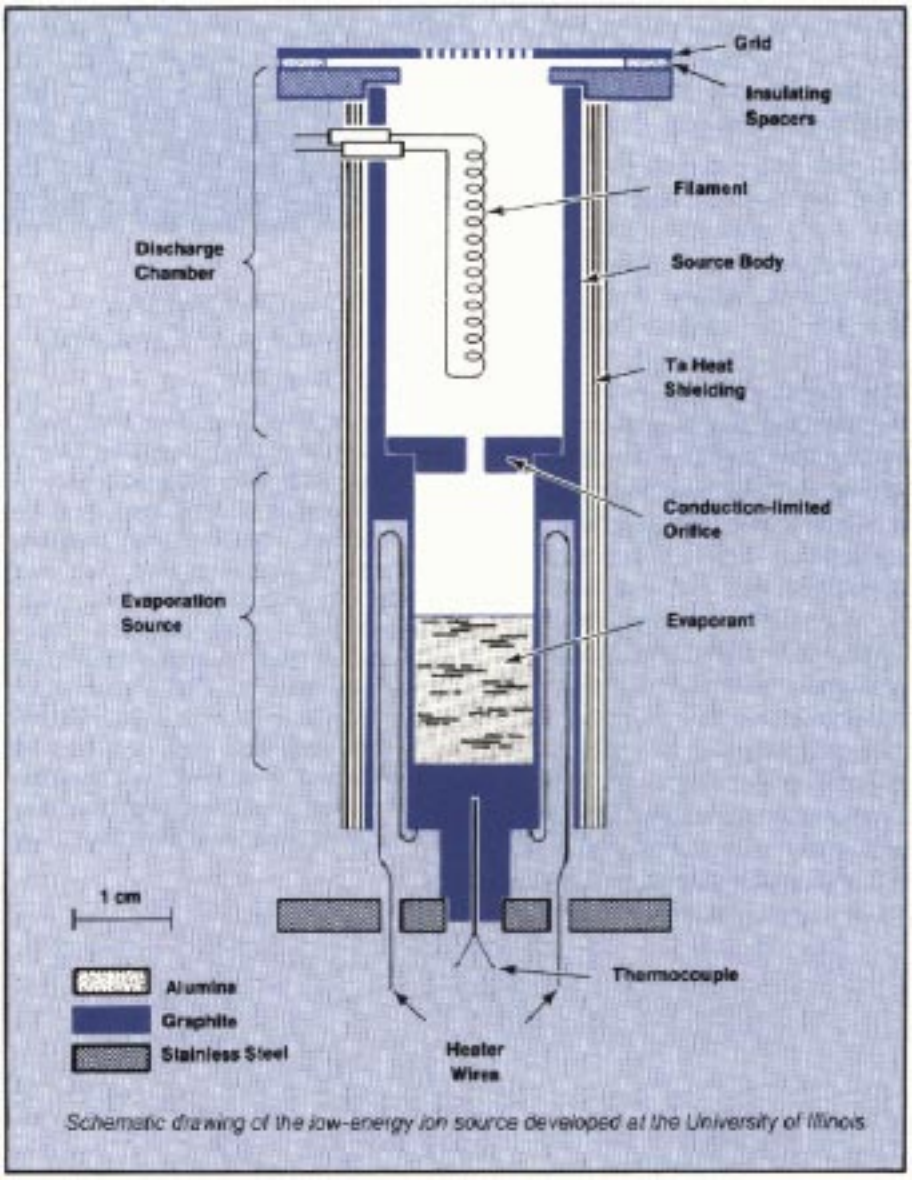
In situ processing, in which the wafer is maintained in a clean controlled environment and processes are brought to the wafer, is the basis for high-yield, short-cycle-time integrated circuit fabrication. This technique has the flexibility to economically address the requirements associated with ASIC designs, i.e., fast-turnaround low-volume production. The SRC in situ processing research thrust emphasizes the use of focused ion beams, rapid thermal processing, and laser beam technology. Research efforts that employ MBE and MOCVD techniques, useful for in situ fabrication, are also underway and contributing to the knowledge base. However, the primary thrust of these latter techniques is toward the advancement of specific device capabilities rather than in situ processes per se.

A Vacuum Generators' Focused Ion Beam (FIB) machine has been recently installed at Rensselaer Polytechnic Institute to provide a direct-write capability. A steered laser beam system for selective etching and deposition for isolation and interconnect research is in operation at Columbia. Controlled doping of epitaxial films has been investigated at Illinois. Lawerence Livermore National Laboratory, Stanford, and XMR, Incorporated (member of SRC SEMI Chapter) are collaborating on steered laser beam interconnection of gate arrays and the use of excimer lasers for MOS device fabrication. Recent results have demonstrated the usefulness of excimer lasers for planarization of metal interconnect and for the formation of shallow (150 nm) source/drain junctions for MOSFETs. Rapid thermal processing (RTP) for thin oxide growth has been developed at Cornell, and RTP for shallow source/drain formation with ion beam mixing is being investigated at Texas.

Controlled Doping in Electronic Thin Films

Fabrication of modern microelectronic and optoelectronic devices requires precise control of doping concentrations and geometries. Ultra-high vacuum compatible ion sources for producing accelerated (rather than the usual thermal energy) dopant beams from gas, liquid, or solid sources at very low energies, 20 to 200 eV, have been developed. The new ion guns can be mounted on standard vacuum flanges in molecular beam epitaxy (MBE), sputter deposition, or plasma-assisted chemical vapor deposition systems. Experiments carried out with a variety of dopants in both silicon and gallium arsenide films grown by MBE and sputter deposition have demonstrated increases in dopant incorporation probabilities by up to 10 orders of magnitude. In addition, a corresponding decrease (more than 2000 angstroms in some cases) in the amount of segregation-induced profile broadening has been observed. A computer code has also been developed for predicting thermal and accelerated-beam dopant distributions as a function of film growth parameters. These results are quite general in nature and are expected to lead to much greater flexibility in designing and fabricating the next generation of electronic devices.

SRC Contract 82-11-006
University of Illinois at Urbana-Champaign
Professor J. E. Greene,
Principal Investigator

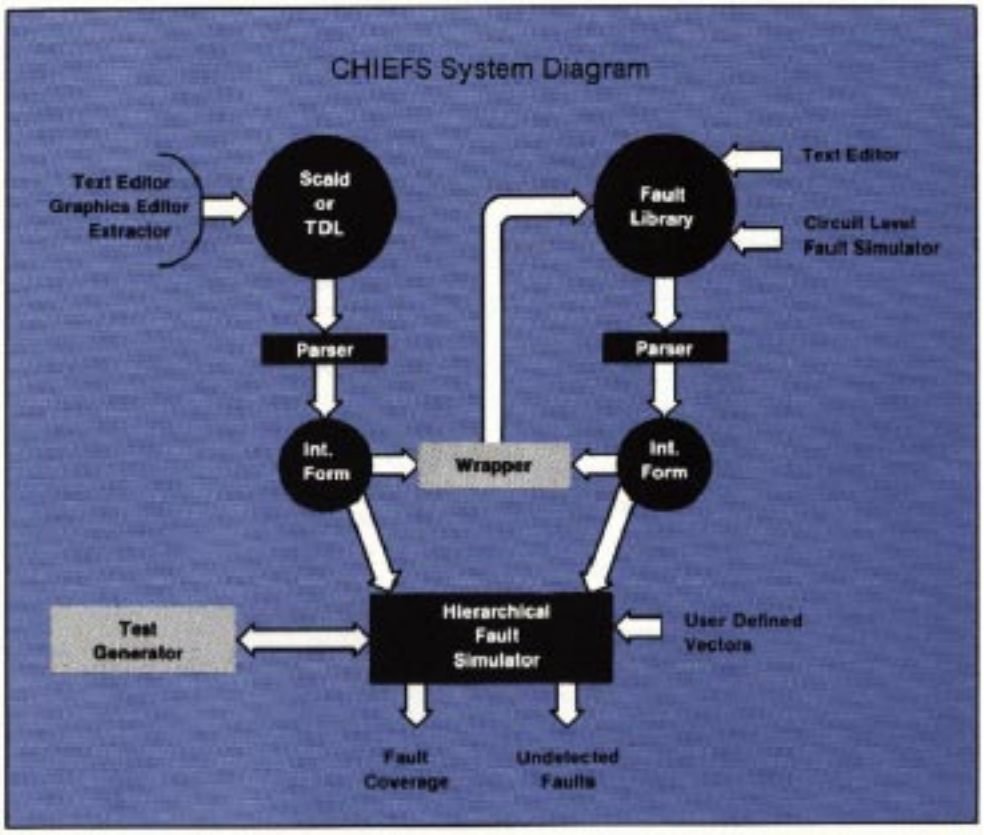


Schematic drawing of the low-energy ion source developed at the University of Illinois

Design for Testability and Reliability

A radically new approach to circuit verification and fault simulation at Carnegie-Mellon accepts as input data the switch-level representation of a MOS circuit. The program, MOSSYM, computes the symbolic input/output relationships for the given circuit. MOSSYM allows the user to inject circuit faults and computes the faulted symbolic behavior of the circuit. An additional feature of this program is that it can be used to compute test vectors for sequential and for combinational circuits. In many cases, particularly those with high input/output count, the performance of MOSSYM appears to be superior to that of conventional input/output response methods for verifying circuit behavior.

Increases in the complexity of VLSI systems create a corresponding increase in the need for sophisticated algorithm-level methods to detect and correct internal system failures. An approach to this problem has been developed at the University of Illinois that has broad applicability for highly structured signalprocessing and linear algebra problems. The central idea is to exploit regularity by including a form of checksum encoding in the architecture by the addition of O(1/N) processors, where N is the size of the processing array. The problem of reconfiguring a highly parallel architecture, containing spare elements when one of the links or processing elements has failed, has also been addressed at Illinois; and strategies for reconfiguration have been developed for some of the most popular communication structures, including the Shuffle Exchange and the Chain-Structured Butterfly Processor.



CHIEFS: A Concurrent, Hierarchical, and Extensible Fault Simulator

As IC designs get larger, one of the major activities in the design process, fault simulation, requires significantly greater computational resources. CHIEFS, the fault simulator developed at the University of Illinois, addresses this problem by using the circuit hierarchy to reconfigure the circuit and perform a hierarchically partitioned multipass simulation that effectively reduces the number of modules. CHIEFS simulates directly from a hierarchical circuit description without flattening the circuit to the level of primitives. The simulator is decoupled from the fault model and supports user-extensible fault libraries and interfaces. The library can represent any fault with a logically modeled effect, and it is possible to interface to functional descriptions of modules, allowing a mixed-mode simulation. This, in turn, allows fault simulation to begin earlier in the design process and, thus, reduces the length of the overall design time. Performance measurements on circuits with up to 30,000 faults have shown speedups of up to 60 times over nonpartitioned simulation. The techniques used in CHIEFS should help contain design time and cost by permitting faster, more cost-effective fault simulation.

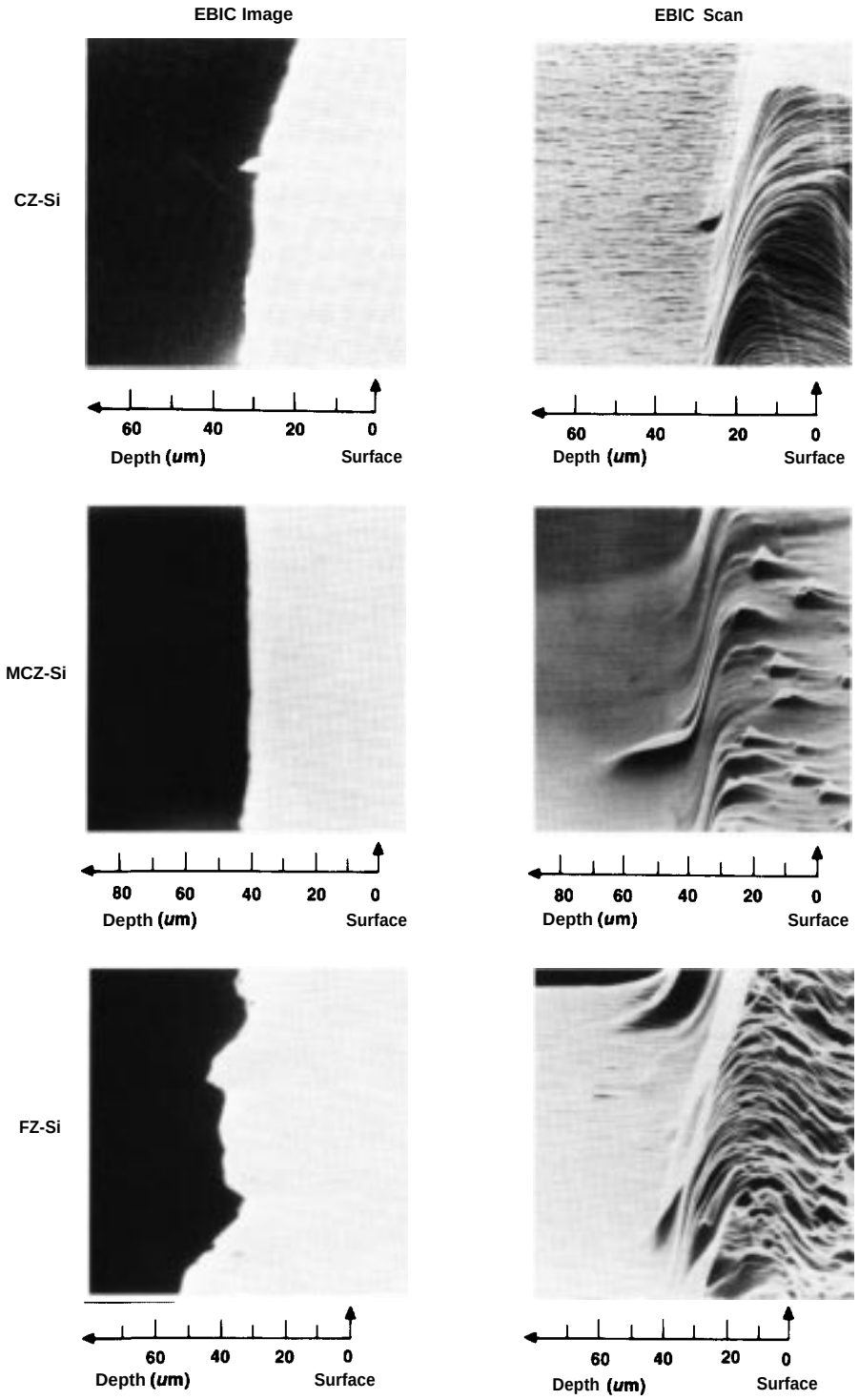
SRC Contract 84-06-049
University of Illinois at Urbana/Champaign
Professor J.A. Abraham,
Program Director

Intrinsic Gettering in Oxygen- Free Silicon

Intrinsic gettering is commonly used in silicon IC technology in order to outdiffuse defects from the device-active surface region of the wafer by high temperature treatment (formation of the denuded zone). The presence of oxygen has been essential in order to form oxide precipitates below the device region which getter the metallic contaminants from the denuded zone. Accordingly, oxygen-free silicon crystals or crystals grown in the low oxygen concentrations of magnetic fields could not be used in IC technology. investigations are being conducted with a new intrinsic gettering process that results in the formation of a denuded zone in silicon crystals with both intermediate and very low concentrations of oxygen. A mode/ is being developed that involves outdiffusion and precipitation of silicon interstitials to permit the use of float-zone-grown silicon crystals and Czochralski-pulled crystals in the presence of magnetic fields. These types of crystals often present distinct advantages (lower level of background impurities and better homogeneity) over those commonly used in IC technology.

SRC Contract 83-12-043
Massachusetts Institute of Technology

Professor Harry C. Gatos,
Principal Investigator



Denuded zones as revealed by minority carrier lifetimes in three types of heat-treated Si crystals: CZ (ordinary Czochralski), MCZ (Czochralski in the presence of magnetic fields), and FZ (float-zone-grown). Both images and scans of EBIC (electron beam-induced current) are shown as obtained by scanning electron microscopy. The white surface region in the images indicates high values of lifetimes, whereas the dark region below the denuded zone indicates very low values of lifetime (due to precipitates). Similarly, the scans indicate high values of EBIC in the surface region which decrease abruptly below the denuded zone.

New Directions

The future directions for the SRC research program are defined by the goals and research objectives. Functions for the SRC that are separate from the research agenda have been addressed by both the Technical Advisory Board and the Board of Directors and are embodied in the SRC Long Range Plan.

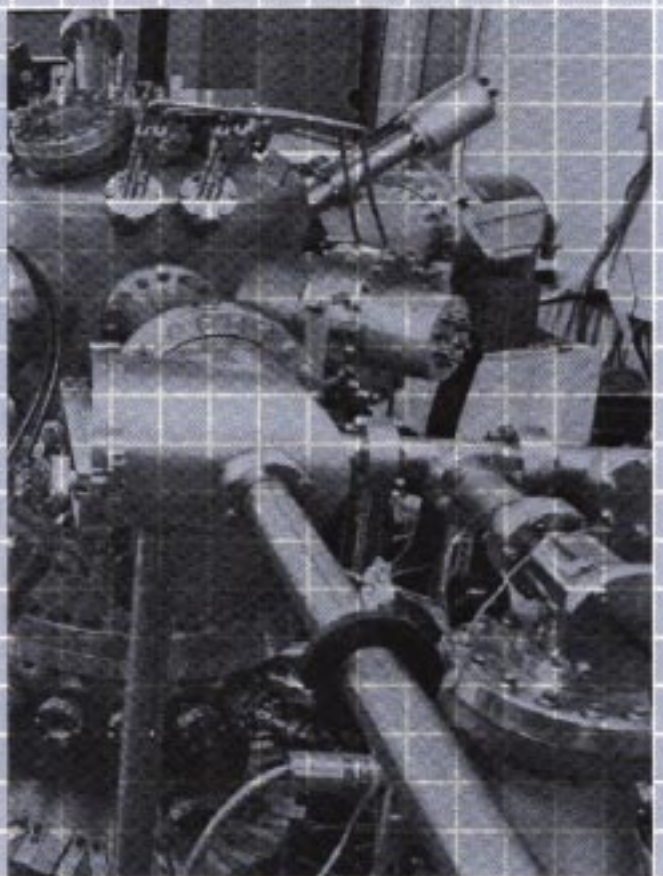
The SRC Long Range Plan calls for new activities that are extensions of the basic research program. Several such initiatives have been undertaken in the past year that respond to this directive. This includes the fellowship program, the manufacturing education initiative, technology assessment, the Manufacturing Competitiveness Panel, and information gathering. It is expected that these activities will be strengthened in the future and that other initiatives will be explored that provide advantages to member companies. The fellowship program is described earlier in this report.

Manufacturing Education

This initiative addresses the need for engineers skilled in semiconductor manufacturing science. At Florida State University, under contract to the SRC, an interdisciplinary team (consisting of electrical, chemical, and mechanical engineering department chairmen; the chairman of the solid state physics group; and an SRC representative) are determining, through industry interactions, the desired attributes of a curriculum for semiconductor manufacturing engineers. Projection of the image of manufacturing as a needed and attractive career option for engineers in both the academic and industrial communities is being studied.

Technology Assessment

An assessment of Japanese capabilities in memory, gate array, and bipolar integrated circuits was undertaken in a workshop. The primary participants represented SRC member companies. Specific reported technical advances were evaluated and compared to U.S. technology. It was concluded that, in general, these competitors to U.S. companies did not have any advantage in technological knowledge but were superior performers in implementation and follow-through based upon this knowledge. This workshop illustrated an increased willingness on the part of the U.S. industry to exchange information and participate in joint analyses of common issues.



Manufacturing Competitiveness

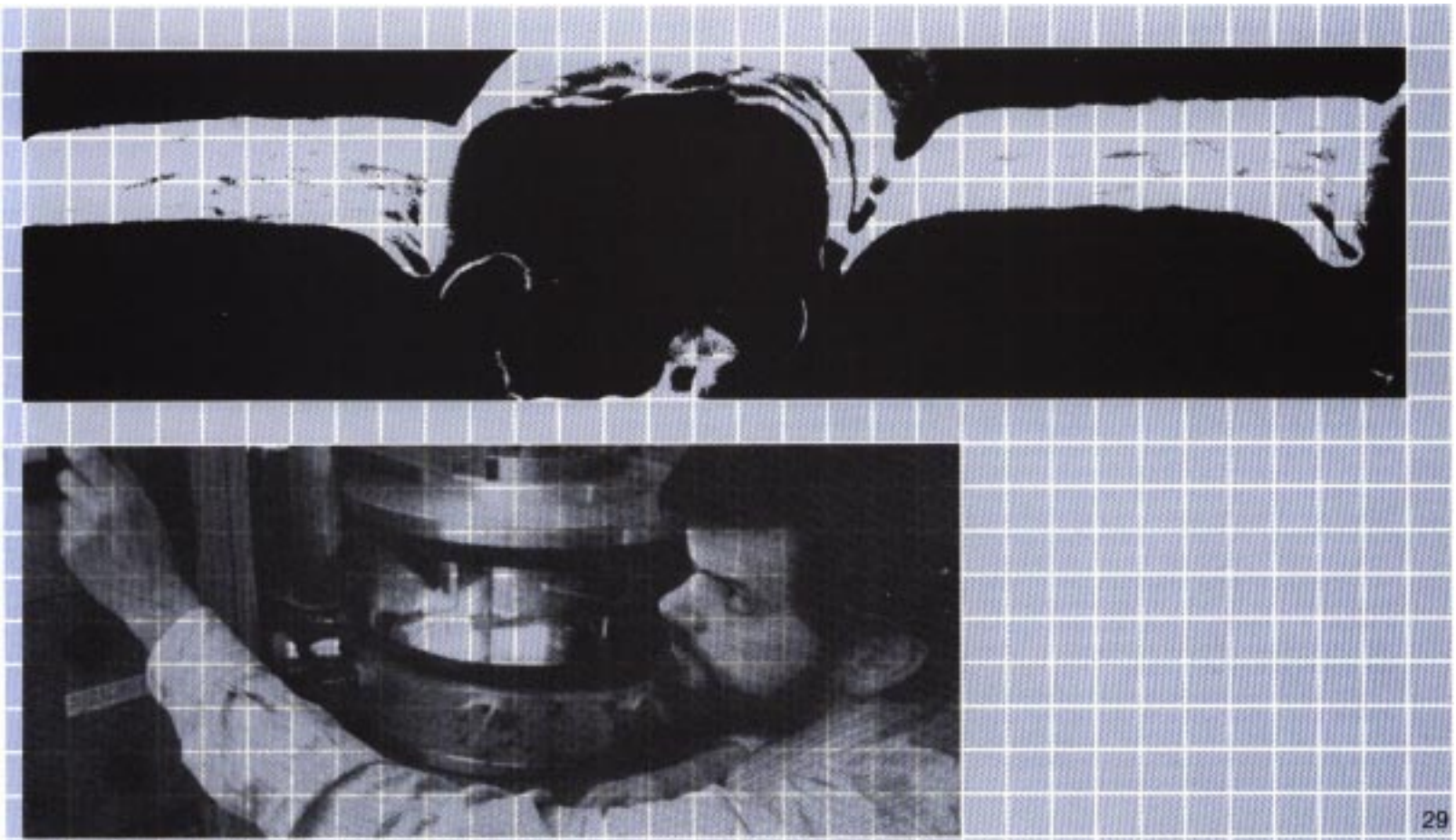
Another issue that concerns a number of SRC members relates to the competitive threat to the U.S. semiconductor manufacturing equipment industry. To address this issue, a panel was organized under the aegis of the TAB Manufacturing Sciences Committee. In a series of meetings, equipment-related problems were discussed and several innovative solutions were proposed. One example is the evolution of a protocol for improved communications between the builders and users of the equipment to promote better products.

Information Collection

This activity has been limited, to date, to the opportunistic acquisition of reports on foreign technology. Consideration is being given to the establishment of electronically accessible data bases on research activities related to the SRC agenda and other information of interest to the industry being served.

These extensions beyond the core research program of the SRC are being classified as industry support activities. At present, these comprise less than five percent of the SRC program. They are expected to increase, but will always be a relatively small portion of the total effort.

The SRC has demonstrated cooperation in support and direction of academic research and is exploring other cooperative activities. A II persons involved in this effort are aware that these measures will alleviate, but not solve, the fundamental competitive problems of the industry for which the SRC was founded. However, SRC companies, working with the larger community, will continue to explore options for cooperation that address these larger problems, and cooperative solutions will be found.



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